MODIFICATION HISTORY

MODEL NAME : KE-P37XS1/P42XS1
KE-MX42A1/MX42S1/MX42M1
KDE-P37XS1/P42XS1

SERVICE MANUAL

PARTS No. : 9-878-248-02

* Blue characters are linking.

No.	DATA	CONTENTS
1	2004. 6	Addition of Hong Kong, ME, China, OCE and UK Models. Correction of The Parts Information. (P.83)

KE-P37XS1/P42XS1
KDE-P37XS1/P42XS1
KE-MX42A1/MX42S1/MX42M1

PANEL MODULE SERVICE MANUAL

PDP Module Name

FPF37C128128UB
FPF42C128128UC

KE-P37XS1	*AEP Model*
KE-P42XS1	*AEP Model*
KDE-P37XS1	*UK Model*
KDE-P42XS1	*UK Model*
KE-MX42A1	*Hong Kong Model*
KE-MX42A1	*ME Model*
KE-MX42M1	*China Model*
KE-MX42S1	*OCE Model*

FLAT PANEL COLOR TV

SONY®

CONTENTS

Scope; 42A1 series

(Model name; FPF42C128128UC)

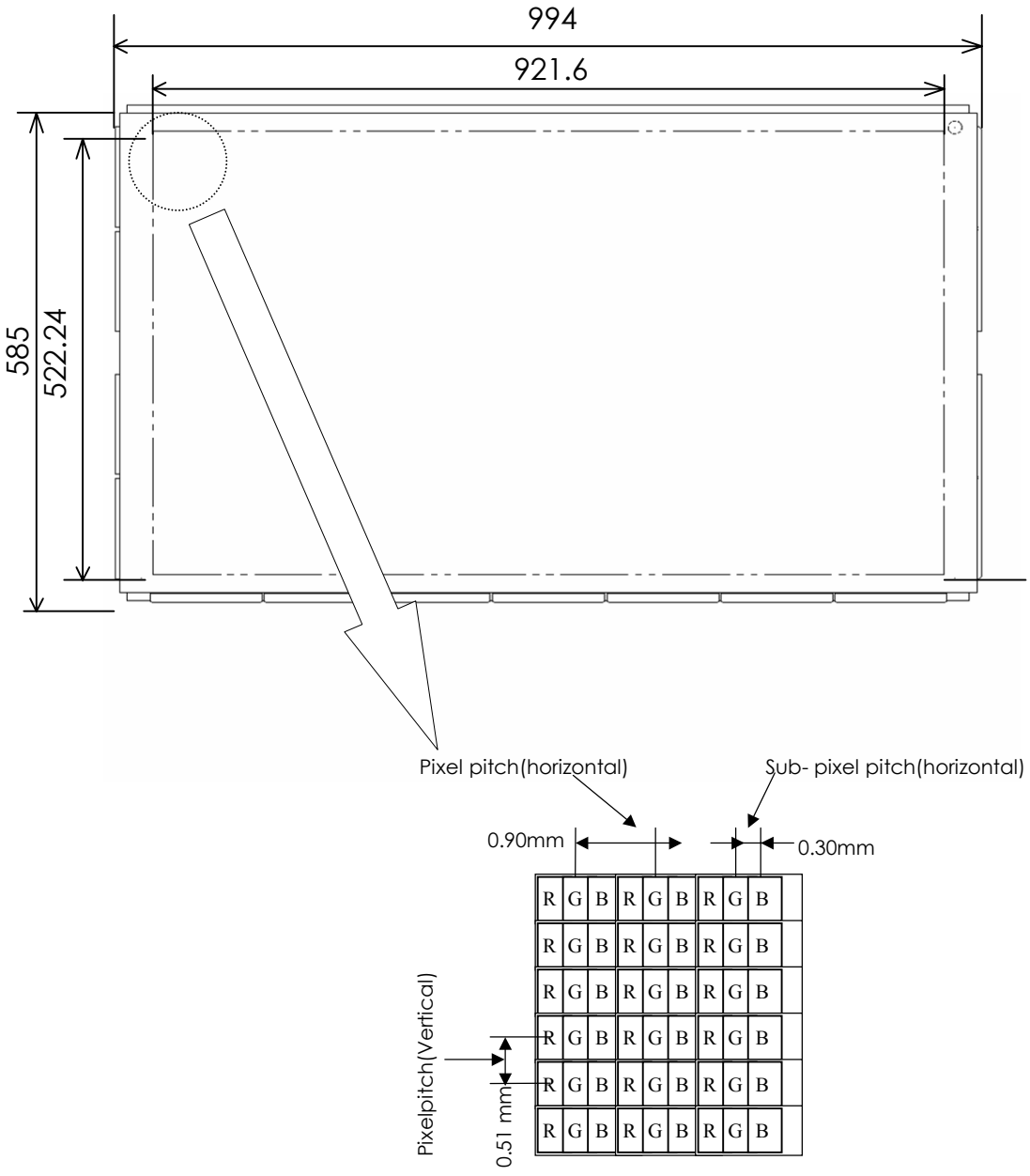
Caution

Before doing the service operation please be sure to read this service analysis manual. This module has a lot of devices to secure the safety against the fire, electric shock, injury and harmful radiation.
To maintain the safety control, please follow the instructions and remarks described in this service analysis manual.

1 OUTLINE

The module is a plasma display module which can be designed in there is no fan in addition to a general feature of the plasma display such as a flat type, lightness, and high-viewing-angle and terrestrial magnetism.

1.1 PANEL DIMENSION



1.2 FEATURE

1. For high definition television by ALIS method
2. For FAN Less design(Low consumption electric power)
3. Flat type・Lightness
4. Customizing of module equipped with communication function

1.3 SPECIFICATION

1.3.1 Functional specification

Item		NO	Specification
			UC-5X
Externals	Module size	1	994 × 585 × 66mm
	Weight	2	16kg
Display panel	Display size	3	921.60 × 522.24mm (42inch: 16:9)
	Resolution	4	1024 × 1024 pixel
	Pixel pitch	5	0.90(H) × 0.51(V)mm
	Sub pixel pitch	6	0.30(H) × 0.51(V)mm
Color	Grayscale(standard)	7	RGB each color 256 Grayscale
BrightNess	White(display load Ratio 100%)	8	140cd/ m^2
	White(display load Ratio 1%,standard)	9	(1000) cd/ m^2
Chromaticity Coordinates	(x,y)、white 10%	10	(0.300,0.300)
Contrast	Contrast in Darkroom(60Hz)	11	(1000:1)
Data signal	Video signal (RGB each color)	12	LVDS(10bit)
	Dot clock(max)	13	52MHz
Sync Signal	Horizontal Sync Signal(max)	14	50KHz(LVDS)
	Vertical Sync Signal	15	50Hz ± 1.9 / 60 ± 1.7Hz (LVDS)
Powersupply	Input voltage/current	16	+3.3/+5/+75-90/+50-65V_{DC}, 0.05/6/4/2A
	Standby electric power(max)	17	1W
Noise	Shade noise at 18dB(A) or less	18	25dB(A) or less
Guarantee environment	Temperature(operation)	19	0 ~ 45 °C
	Temperature(storage)	20	0 ~ 45 °C
	Humidity(operation)	21	20 ~ 85 %RH (no condensation)
	Humidity(storage)	22	20 ~ 80 %RH (no condensation)

***It is made to give priority when there is a delivery specification according to the customer.**

1.3.2 Display quality specification

Item		NO	Specification
			UC-51 (Standard)
Non-lighting cell defect	Total number (subpixel)	1	15 or less
	Density (subpixel/cm^2)	2	2 or less （However,1 continuousness or less）
	Size (H x V) (subpixel)	3	1x2 or less, Or 2x1 or less
Non-extinguishing cell defect	Total number (subpixel)	4	6 or less（each color 2 or less）
	Density (subpixel/ cm^2)	5	Each color 2 cells max （However,1 continuousness or less）
Flickering cell defect	Flickering lighting cell defect (sub pixel/cm^2)	6	5 or less
	Flickering non-extinguishing cell defect	7	Number on inside of Non-extinguishing cell defect
High intensity cell defect	Twice or more bright point	8	0
Brightness variation	White block of 10% load [9 point] (%)	9	20 or less
	In area adjacent 20mm [White] (%)	10	10 or less
Color variation	White block of 10% load [9 point]	11	X: Average ± 0.015 y: Average ± 0.015

***It is made to give priority when there is a delivery specification according to the customer.**

1.3.3 I/O Interface Specification

(1) I/O Signal

No.	Item	Signal Name		Number of signals	I/O	Form	Content of definition
1	Display data	Video Signal Timing Signal	RA- RA+ RB- RB+ RC- RC+ RD- RD+ RE- RE+	1 1 1 1 1 1 1 1 1 1	Input	LVDS Differential	Differential serial data signal. Input video and timing signals after differential serial conversion using a dedicated transceiver. The serial data signal is transmitted seven times faster than the base signal.
		Clock	RXCLKIN- RXCLKIN+	1 1	Input	LVDS Differential	Differential clock signal. Input the clock signal after differential conversion using a dedicated transceiver. The clock signal is transmitted at the same speed as the base signal.
		Power down Signal	PDWN	1	Input	LVTTL	Low :LVDS receiver outputs are all "L". High: Input signals are active.
2	MPU Communication / Control	Communication	SDA	1	I/O	LVTTL (I^2C)	I^2C bus serial data communication signal. Communication with the control MPU of this product is enabled.
			SCL	1	I/O		
		Control	CPUGO	1	Input	LVTTL	Low power consumption mode of the control MPU of this product is released.
			PDPGO	1	Input	LVTTL	"High": This product is started. (CPUGO="High" Effective)
			IRQ	1	Output	LVTTL	It changes into "Low" → "High" when this product enters the undermentioned state. 1. Vcc/Va/Vs output decrease 2. Circuit abnormality detection

(2) LVDS Signal Definition and Function

A video signal (display data signal and control signal) is converted from parallel data to serial data with the LVDS transmitter and further converted into four sets of differential signals before input to this product.

These signals are transmitted seven times faster than dot clock signals.

The dot clock signal is converted into one set of differential signals by the transmitter before input to this product.

The LVDS signal definition and function are summarized below:

Signal name	Symbol	Number of signals	Signal definition and function
Video signal Timing signal Transmission line	RA- RA+	1 1	Display data signal R2, R3, R4, R5, R6, R7, G2
	RB- RB+	1 1	Display data signal G3, G4, G5, G6, G7, B2 B4
	RC- RC+	1 1	Display data signal, Sync Signal, Control signal B4, B5, B6, B7, $\overline{\text{Hsync}}$, $\overline{\text{Vsync}}$, $\overline{\text{BLANK}}$
	RD- RD+	1 1	Display data signal, Control signal R8, R9, G8, G9, B8, B9, PARITY
	RE- RE+	1 1	Display data signal, Control signal R0, R1, G0, G1, B0, B1, N.S
Clock transmission line	RXCLKIN- RXCLKIN+	1 1	Clock signal $\overline{\text{DCLK}}$

(3) Video Signal Definition and Function

The table below summarizes the definitions and functions of input video signals before LVDS conversion.

Item	Signal name		Number of signals	Input/ output	Signal definition and function
Original Display signal (before LVDS transmittance)	Video signal (digital RGB)	DATA-R DATA-G DATA-B	10 10 10	Input	Display data signal R9/G9/B9 is the highest intensity bit. R0/G0/B0 is the lowest intensity bit.
	Data Clock	$\overline{\text{DCLK}}$	1	Input	Display data timing signal: Data are read when $\overline{\text{DCLK}}$ is lowerd. $\overline{\text{DCLK}}$ is continuously input.
	Horizontal sync signal	$\overline{\text{Hsync}}$	1	Input	Regulates one horizontal line of data: Begins control of the next screen when $\overline{\text{Hsync}}$ is lowered.
	Vertical sync signal	$\overline{\text{Vsync}}$	1	Input	Screen starts up control timing signal: Begins control of the next screen when $\overline{\text{Vsync}}$ is lowered. Input the same frequency in both odd-numbered and even-numbered fields.
	Parity signal	PARITY	1	Input	This signal specifies the display field. H: Odd-numbered field L: Even-numbered field Parity signal should be alternated in every $\overline{\text{Vsync}}$ cycle.
	Blanking signal	$\overline{\text{BLANK}}$	1	Input	Display period timing signal. H indicates the display period and L indicates the non display period. Note: Set this timing properly like followings, as is used internally for signal processing. ・Set the blanking period so that the number of effective display data items in one horizontal period is 1024. ・Set the number of blanking signals in one vertical period to 512, which is one half the number of effective scan lines. If the $\overline{\text{BLANK}}$ changes when the $\overline{\text{Vsync}}$ frequency is switched, the screen display may be disturbed or brightness may change. The screen display is restored to the normal state later when the $\overline{\text{BLANK}}$ length is constant again.

***This product does not correspond to the progressive display mode by the parity signal fixation. When the parity signal is fixed, this product is reversed arbitrarily internally and used.**

1.3.4 Connector Specifications

The connector specification is shown below. Please do not connect anything with the terminal NC.

(1) Signal connector [CN1]

Pin No.	Signal name	Pin No.	Signal name
1	RA-	2	GND(LVDS)
3	RA+	4	SCL
5	RB-	6	GND
7	RB+	8	SDA
9	RC-	10	GND(LVDS)
11	RC+	12	CPUGO
13	RXCLKIN-	14	PDPGO
15	RXCLKIN+	16	IRQ
17	RD-	18	PDWN
19	RD+	20	GND(LVDS)
21	RE-	22	GND
23	RE+	24	GND
25	GND	26	GND
27	GND	28	GND
29	GND	30	GND

DF13-30DP-1.25 V (tin-plated) (Maker: HIROSE DENKI)

[Conforming connector] *Housing: DF13-30DS-1.25C*
Contact: DF13-2630SCF

(2) Power Source Connectors (PSU only is used on repair working)

(a) Power input connector [CN61]

Pin No.	Symbol
1	AC(L)
2	N.C
3	AC(N)
4	N.C
5	N.C
6	F.G

B06P-VH (Maker: JST)

[Conforming connector]
Housing: VHR-06N(or M)
Contact: SVH-21T-P1.1

(b) Power supply output connector for system [CN62]

Pin No.	Symbol
1	V_{AUX}
2	N.C
3	GND

B03P-VH (Maker: JST)

[Conforming connector]
Housing: VHR-06N(or M)
*Contact: SVH-*21T-*P1.1*

(c) Power supply output connector for system [CN63]

Pin No.	Symbol
1	Vpr1
2	N.C.
3	Vpr2
4	N.C.
5	GND

B5B-XH-A (Maker: JST)

[*Conforming connector]*
Housing: XHP-5
Contact: SXH-*001T-P0.6*

(iii) Power Source Connectors

(a) Power supply output connector for system [CN6]

Pin No.	Symbol
1	Vpr2
2	N.C.
3	GND
4	GND
5	N.C.
6	Vcc

B6B-PH-SM3(JST)

[Conforming connector]
Housing: PHR-6
Contact: SPH-002T-P0.5L

(b) [CN23]

Pin No.	Symbol
1	Va
2	N.C.
3	Vcc
4	GND
5	GND
6	GND
7	N.C.
8	Vs
9	Vs
10	Vs

B10P-VH(JST)

[Conforming connector]
Housing: VHR-10N
Contact: SVH-21T-P1.1

(c) Power supply output connector for system [CN7]

Pin No.	Symbol	Pin No.	Symbol
1	N.C.	11	GND
2	N.C.	12	Vra
3	N.C.	13	GND
4	N.C.	14	Vrs
5	GND	15	GND
6	VSAGO	16	Iak
7	GND	17	GND
8	VCEGO	18	Vak
9	GND	19	GND
10	PFCGO	20	Vsk

00 6200 520 330 000 [ZIF Right Angle Connector] (Kyocera elco)

2 SAFETY HANDLING of THE PLASMA DISPLAY

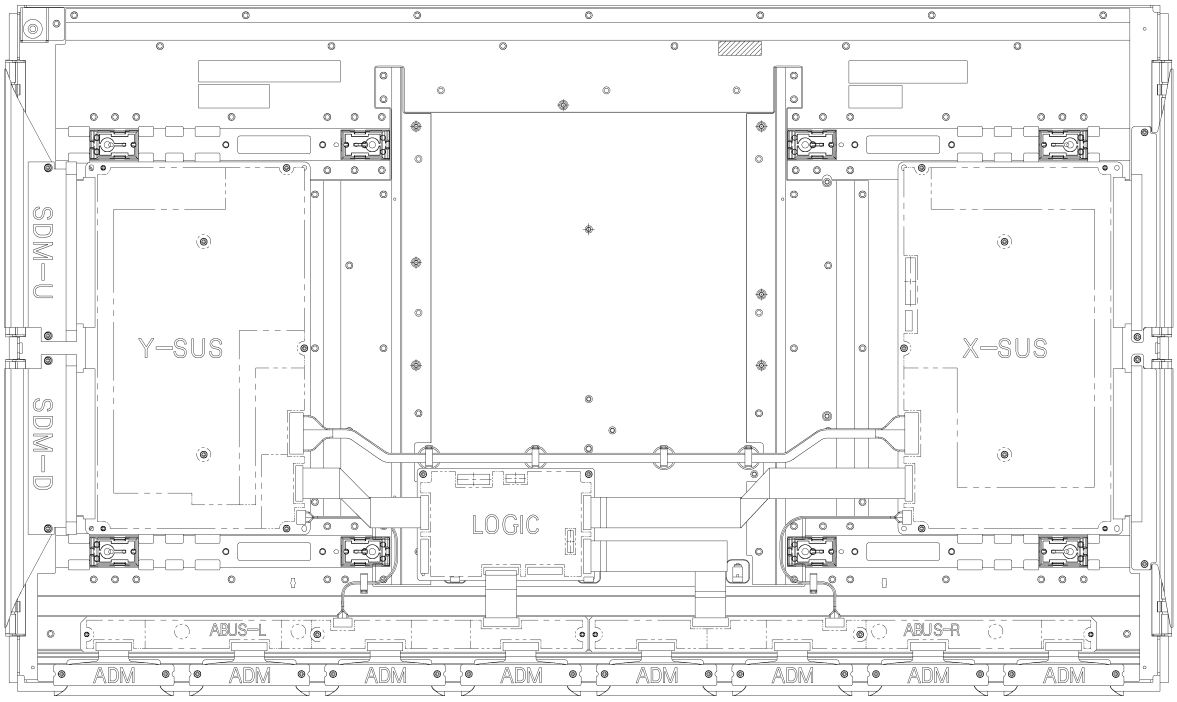
2.1 NOTES TO FOLLOW DURING SERVICING

- The work procedures shown with the Note indication are important for ensuring the safety of the product and the servicing work. Be sure to follow these instructions.
- Before starting the work, secure a sufficient working space.
- At all times other than when adjusting and checking the product, be sure to turn OFF the main POWER switch and disconnect the power cable from the power source of the display (jig or the display itself) during servicing.
- To prevent electric shock and breakage of PC board, start the servicing work at least 30 seconds after the main power has been turned off. Especially when installing and removing the power supply PC board and the SUS PC board in which high voltages are applied, start servicing at least 2 minutes after the main power has been turned off.
- While the main power is on, do not touch any parts or circuits other than the ones specified. The high voltage power supply block within the PDP module has a floating ground. If any connection other than the one specified is made between the measuring equipment and the high voltage power supply block, it can result in electric shock or activation of the leakage-detection circuit breaker.
- When installing the PDP module in, and removing it from the packing carton, be sure to have at least two persons perform the work while being careful to ensure that the flexible printed-circuit cable of the PDP module does not get caught by the packing carton.
- When the surface of the panel comes into contact with the cushioning materials, be sure to confirm that there is no foreign matter on top of the cushioning materials before the surface of the panel comes into contact with the cushioning materials. Failure to observe this precaution may result in the surface of the panel being scratched by foreign matter.
- When handling the circuit PC board, be sure to remove static electricity from your body before handling the circuit PC board.
- Be sure to handle the circuit PC board by holding the such large parts as the heat sink or transformer. Failure to observe this precaution may result in the occurrence of an abnormality in the soldered areas.
- Do not stack the circuit PC boards.
  Failure to observe this precaution may result in problems resulting from scratches on the parts, the deformation of parts, and short-circuits due to residual electric charge.
- Routing of the wires and fixing them in position must be done in accordance with the original routing and fixing configuration when servicing is completed.
  All the wires are routed far away from the areas that become hot (such as the heat sink). These wires are fixed in position with the wire clamps so that the wires do not move, thereby ensuring that they are not damaged and their materials do not deteriorate over long periods of time. Therefore, route the cables and fix the cables to the original position and states using the wire clamps.
- Perform a safety check when servicing is completed.
  Verify that the peripherals of the serviced points have not undergone any deterioration during servicing. Also verify that the screws, parts and cables removed for servicing purposes have all been returned to their proper locations in accordance with the original setup.

3 NAME and FUNCTION

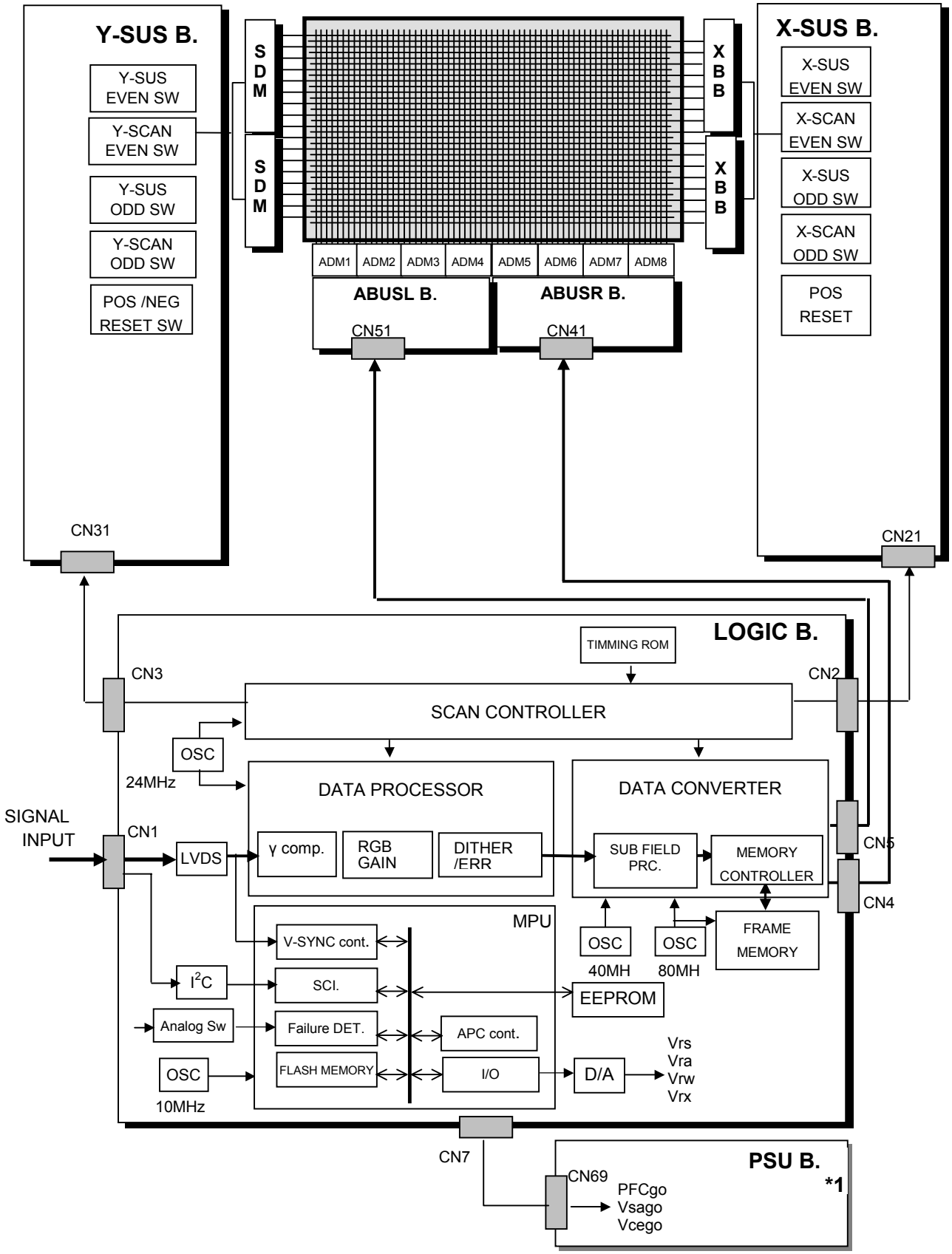
3.1 CONFIGURATION

(1) FPF42C128128UC-53 (LOGIC set out left side)

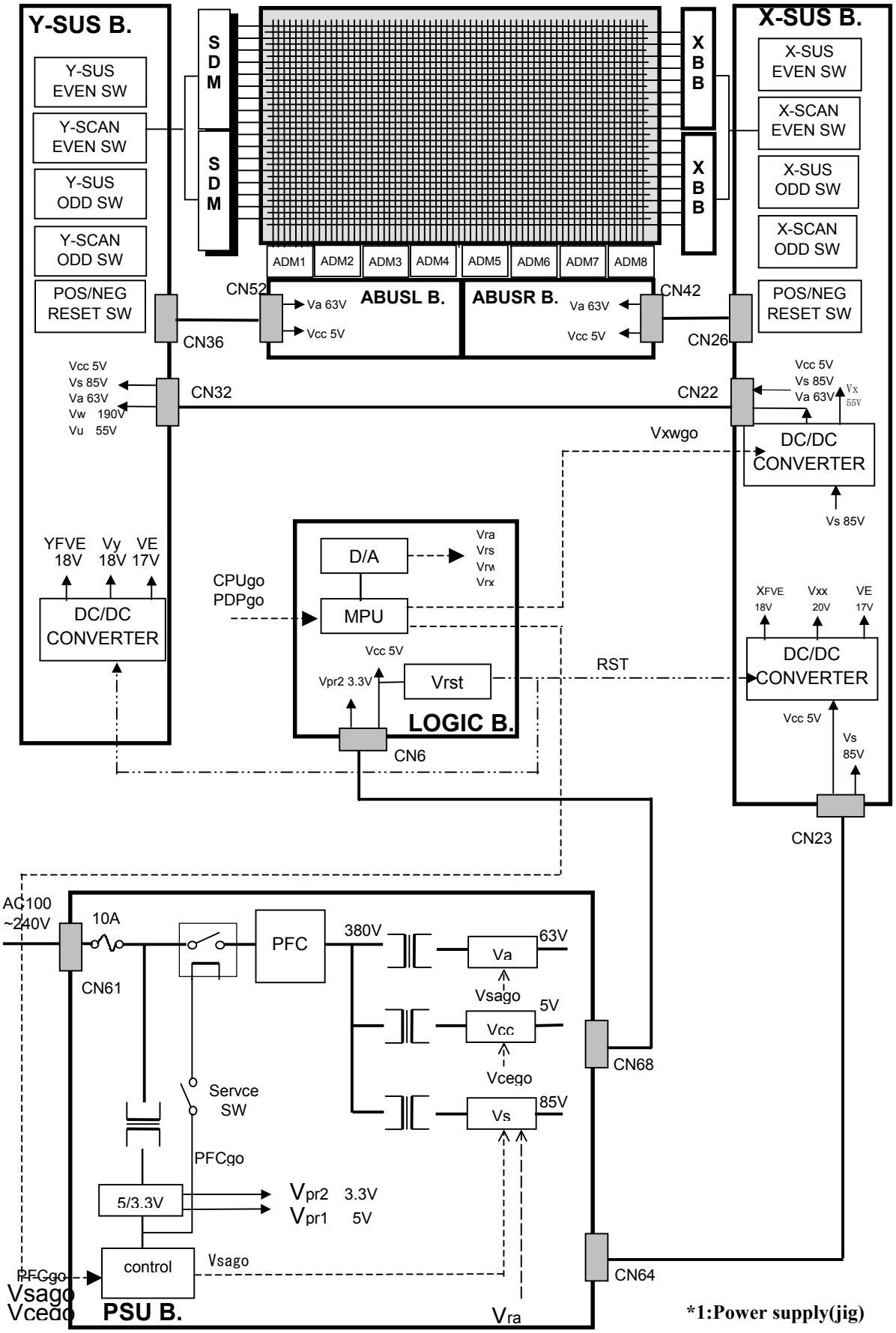


3.2 BLOCK DIAGRAMS

3.2.1 Signal Diagrams



3.2.2 Power Diagrams



3.3 FUNCTION

3.3.1 Logic board Function

(1) Data Processor

- γ adjustment(1 / 2.2 / 2.4 / 2.6 / 2.8)
- NTSC/EBU format(Color matrix) Switch
- RGB gain Control(White balance adjustment, Amplitude limitation)
- Error Diffusion Technology(Grayscale adjustment)
- Dither(Grayscale adjustment)
- Burn-in Pattern generation

(2) Data Converter

- Quasi out-line adjustment (luminous pattern control)

(3) Scan Controller

- Address driver control signal generator(ADM)
- scan driver control signal generator(SDM)
- X/Y sustain control signal generator

(4) Waveform ROM

- Waveform Pattern for drive / Timing memory

(5) MPU

- Synchronous detection
- System control
- Driving voltage(Va, Vs, Vr, Vw) Minute adjustment
- Abnormal watch (breakdown detection)/abnormal processing
- Is(sustain) current control (sustain pulse control)
- Ia(address) current control (sub-field control)
- External communication control
- Flash memory (firmware)

(6) EEPROM

- Control parameter memory
- The accumulation energizing time (Every hour).
- Abnormal status memory (16 careers)

Sub Address	Data bit	Symbol	Item	Function	Setting [hex]	
					RANGE	INITIAL value
00	7-0	MAPVER	address MAP VERsion	Indicates the version number of the address map.	00 ~ FF	01
01	7	ERRF	update of ERRor Flag	Indicates that an error has occurred. It can be cleared with the ErrRST setting. If this flag is set, Error code is written. Cannot enter the PDP-ON mode.	0: Not updated 1: Updated	0
	6	OHRF	update of Operation HouRs Flag	Indicates that the drive hours are counted.	0: Not updated 1: Updated	0
	5	PSDF	Power Shut Down Flag	Indicates that shutdown of the AC power is detected and the PDP has executed the OFF-sequence. It can be cleared with the PSDRST setting.	0: Not detected 1: Detected	0
	4-0	CNDC	CoNDition Code	Indicates status of the module.	Refer to 4.11.2.6 condition codes.	Irregular
02	7-0	ERRC	ERRor Code	Indicates error code. The error codes of as many as 16 errors in the past can be retrieved with the ERRS setting. . Same error code is not stored continuously.	00~FF	00
03	7-0	OHRH	Operation HouRs Higher bits	Indicates the higher 8 bits of the module driving hours.	00~FF	00
04	7-0	OHRL	Operation HouRs Lower bits	Indicates the lower 8 bits of the module driving hours.	00~FF	00

Sub Address	Data bit	Symbol	Item	Function	Setting [hex]	
					RANGE	INITIAL value
20	7	PATSEL	Selecting patterns	It selects the built-in test pattern signals of this display. This setting is valid when the PATON setting is 1.	0: The single color display is switched every 2 seconds. A total of 8 colors are displayed. 1:All white (Different from actual white.)	0
	6	PATON	Built-in pattern display is set to ON.	Display of the built-in pattern signal in this product is turned ON/OFF.	0: Displaying the input signal 1: Displaying the built-in pattern	0
	5	ADEN	Address data enable	The black screen is displayed. 0 is set when the input video signal has disturbance.	0: Blank 1: Displaying the input signal	1
	4	-	-	Be sure to use the display with the setting fixed to 0.	0~1	0
	3	DSPPOL	DiSPlay POLarity	Input reflection polarity setting	0:Emits light by LOW 1:Emits light by High	1
	2	PFCON	forcing PFC ON	When PFCON = 0, If a high voltage power is switched on, PFCGO is set high before a high voltage power is output. When PDPON = 1, PFCGO is set high irrespective of the state of a high voltage power. Use it for a power control when a high voltage power is off.	0: Power OFF 1: Power ON	0
	1	PDPON	High voltage power supply ON	Switches ON/OFF the high voltage power supply of PDP.	0: Power OFF 1: Power ON	0
	0	DSPBIT	Input Data bit	Switches 8 bit input / 10 bit input	0: 10 bit input 1: 8bit input	1

Sub Address	Data bit	Symbol	Item	Function	Setting [hex]	
					RANGE	INITIAL value
21	7-5	-	-	Be sure to use the display with the setting fixed to 0.	0~7	0
	4	CCFMD	Color correction mode	Selecting the color correction modes. Valid when the CCFON setting is 1	0:Luminance has priority. 1:Gradation has priority	0
	3	DCBON	Dynamic Color Balance	Tracking correction of white balance between the high luminance and the low luminance.	0: OFF 1: ON	0
	2	PPAON	Panel Protect Apc function	When a picture with high luminance/small area is displayed for about 3 minutes or longer, the number of pulses is reduced to about 20% at a maximum. This item can be used to reduce panel temperature/extend useful life when the display is used to show a still image.	0: OFF 1: ON	1
	1	APSON	Auto Peak Save function	If a low display load picture (less than 2%) is inputted continuously 3 minutes or more, the brightness is reduced about 50 %.	0: OFF 1: ON	1
	0	DSETEN	Data Set Enable	Whether the register value is reflected to the operating status of this product, selected by this item. The following switch is executed. 0:The received register value is reflected from the next field. 1:The received register value is stored so that the DSET setting is reflected from the next field. (DSET setting: Setting bit 0 of address FF)	0: Invalid 1: Valid	1
22	7	CCFON	Color correction	Color collection process is turned ON/OFF.	0: OFF 1: ON	0
	6	CCFORM	Color correction format	Color collection process is switched. This item is valid when CCFON setting is 1.	0: NTSC 1: EBU	0
	5-3	-	-	Be sure to use the display with the setting fixed to 0.	0~7	0
	2-0	GAMSEL	Selecting the reverse γ correction	Reverse γ correction level is set. The setup 7 is the test mode. Do not select the setup 7. When the setup 6 is selected, setting of the addressed in the range of 31~51 become valid.	0: OFF 1: 1.0 th power 2: 2.2 nd power 3: 2.4 th power 4: 2.6 th power 5: 2.8 th power 6: USER 7: TEST	2

Sub Address	Data bit	Symbol	Item	Function	Setting [hex]	
					RANGE	INITIAL value
23	7-0	CONTrast	Peak luminance	Peak luminance is adjusted. When the display picture load is heavy, the peak luminance is automatically limited.	00~FF	FF
24	7-0	R-RATIO	R ratio	White balance is adjusted. Use the display with at least one item being set to FF (hex).	00~FF	FF
25	7-0	G-RATIO	G ratio		00~FF	FF
26	7-0	B-RATIO	B ratio		00~FF	FF
27	7	IRQRST	Clearing the IRQ output signal	This item implements control to return the IRQ signal from "HIGH" to "Low" level when an error occurs. When this item is set to 1, the IRQ signal is returned to "Low" level.	0: Normal 1: IRQ signal clear	0
	6	ERRRST	Clearing the ERRF flag	This item implements control to return the ERRF flag to 0 when an error occurs. When this item is set to 1, this setting automatically returns to 0 after returning the ERRF flag to 0.	0: Normal 1: ERRFflag clear	0
	5	OHRRST	Clearing the OHRF flag	The control by which the OHRF flag is returned to 0 is done. This setting automatically returns to the state of 0 after returning 0 the ERRF flag when this setting is set to one.	0: Normal 1: OHRF flag clear	0
	4	PSDRST	Clearing the PSDF flag	This item exercise control to return the PSDF flag to 0 when this machine performs the OFF sequence at AC power shutdown. When this item is set to 1, this setting automatically returns to 0 after returning the PSDF flag to 0.	0: Normal 1: PSDF flag clear	0
	3-0	ERRS	Error code selection	When this setting is changed and the ERRC setting is read out, the error contents (as many as 16 errors) of the module that have occurred in the past can be checked. If more than 16 errors have occurred, the error code is updated starting from the oldest error.	0: Latest error 1: Previous error 2: | E: F: Oldest error	0

Sub Address	Data bit	Symbol	Item	Function		Setting [hex]	
						RANGE	INITIAL value
28	7	PWMP	Power Maximam peek control	The PWMAX setting is switched to constant brightness (peak electric power) control. The password setting is necessary to turn on this setting.		When password is set 0:OFF 1:ON	0
	6	-	-	Be sure to use the display with the setting fixed to 0.		0-1	0
	5-4	PWMAX	Maximum power consumption	PWMP=0	Setting of the maximum electric power.	0: -40W 1: -20W 2: ±0W 3: +20W	2
				PWMP=1	Setting of peak electric power. Electric power by which electric power is permitted in addition to improve practical brightness to the maximum electric power set 3:+20W	0: ±0W 1: +20W 2: +30W 3: +40W	
	3-0	-	-	Be sure to use the display with the setting fixed to 0.		0~F	0
29	7-0	PWM PASS	Password of peak electric power setting	Password of peak electric power setting.The password is described to the delivery specifications. When the password setting is normally done, the reading value of the real thing ground becomes 51.		51: Permission of PWMP ON Another: Prohibition	FF
2A	7-0	VRPASS	Password of VRPOL setting	If 'AA" is written, VRPOL setting can be changed.		00~FF	00
2B	7-4	-	-	-		0~F	0
	3-0	RISTIM	RISe TIMe	Setting of wait time for Vs/Va stabilization at the time of start up sequence. Wait time [ms] = 200×Set value (Ma x:3000[ms])		0~F	5
2C	7-0	PsTPW	Ps-Tank PoWer	The maximum electric power setting: The maximum over electric power from +20W	When the amount of an over electric power becomes PsTPW×PsTTM or less at PWMP=1, the control by which brightness is lowered is done.	00-FF	28
2D	7-0	PsTTM	Ps-Tank TiMe	Time which can operate by the maximum over electric power (*10sec)		00-FF	3C

Sub Address	Data bit	Symbol	Item	Function	Setting [hex]	
					RANGE	INITIAL value
30	7-4	-	-	Be sure to use the display with the setting fixed to C.		
	3	VRPOL	Voltage Reference POLarity	Setting of Vrs/Vra output polarity. Set in the following procedures. 1) Write “AA” in the address 2A. 2) Write “0” or “1” in this address. 3) Write other than “AA” in the address 2A.	0: POSI 1:NEGA	0
	2-0	-	-	Be sure to use the display with the setting fixed to 0.		
31	7-0	GAM00	Reverse γ correction DC	Sets the input level that implements the forced 0 [LSB] output.	00~FF	1F
32	7-2	-	<no use>	-	00~FF	00
	1-0	GAM01[9: 8]	Reverse γ coefficient 01	Reverse γ coefficient value is set.		
33	7-0	GAM01[7: 0]		Input Output value of 8 [LSB]	00~FF	04
34	7-3	-	<no use>	-	00~FF	00
	2-0	GAM02[10: 8]	Reverse γ correction 02	Reverse γ coefficient value is set.		
35	7-0	GAM02[7: 0]		Input Output value of 16 [LSB]	00~FF	24
36	7-4	-	<no use>	-	00~FF	00
	3-0	GAM03[11:8]	Reverse γ correction 03	Reverse γ coefficient value is set. Input Output value of 24 [LSB]		
37	7-0	GAM03 [7: 0]			00~FF	58
38	7-4	-	<no use>	-	00~FF	00
	3-0	GAM04[11: 8]	Reverse γ correction 04	Reverse γ coefficient value is set. Input Output value of 32 [LSB]		
39	7-0	GAM04[7: 0]			00~FF	A7
3A	7-5	-	<no use>	-	00~FF	01
	4-0	GAM05[12: 8]	Reverse γ correction 05	Reverse γ coefficient value is set. Input Output value of 40 [LSB]		
3B	7-1	GAM05[7: 1]			00~FF	12
	0	-	<no use>	-		
3C	7-5	-	<no use>	-	00~FF	01
	4-0	GAM06[12: 8]	Reverse γ correction 06	Reverse γ coefficient value is set. Input Output value of 48 [LSB]		
3D	7-1	GAM06[7: 1]			00~FF	9A
	0	-	<no use>	-		
3E	7-5	-	<no use>	-	00~FF	02
	4-0	GAM07[12: 8]	Reverse γ correction 07	Reverse γ coefficient value is set. Input Output value of 56 [LSB]		
3F	7-2	GAM07[7: 2]			00~FF	40
	1-0	-	<no use>	-		

Sub Address	Data bit	Symbol	Item	Function	Setting [hex]	
					RANGE	INITIAL value
40	7-5	-	<no use>	-	00~FF	03
	4-0	GAM08[12: 8]	Reverse γ correction 08	Reverse γ coefficient value is set. Input Output value of 64 [LSB]		
41	7-2	GAM08[7: 2]			00~FF	04
	1-0	-	<no use>	-		
42	7-6	-	<no use>	-	00~FF	04
	5-0	GAM09[13: 8]	Reverse γ correction 09	Reverse γ coefficient value is set. Input Output value of 80 [LSB]		
43	7-4	GAM09[7: 4]			00~FF	F0
	3-0	-	<no use>	-		
44	7-6	-	<no use>	-	00~FF	07
	5-0	GAM11[13: 8]	Reverse γ correction 10	Reverse γ coefficient value is set. Input Output value of 96 [LSB]		
45	7-4	GAM11[7: 4]			00~FF	60
	3-0	-	<no use>	-		
46	7-6	-	<no use>	-	00~FF	0A
	5-0	GAM11[13: 8]	Reverse γ correction 11	Reverse γ coefficient value is set. Input Output value of 112 [LSB]		
47	7-4	GAM11[7: 4]			00~FF	50
	3-0	-	<no use>	-		
48	7-6	-	<no use>	-	00~FF	0D
	5-0	GAM12[13: 8]	Reverse γ correction 12	Reverse γ coefficient value is set. Input Output value of 128 [LSB]		
49	7-4	GAM12[7: 4]			00~FF	D0
	3-0	-	<no use>	-		
4A	7-6	-	<no use>	-	00~FF	16
	5-0	GAM13[13: 8]	Reverse γ correction 13	Reverse γ coefficient value is set. Input Output value of 160 [LSB]		
4B	7-4	GAM13[7: 4]			00~FF	A0
	3-0	-	<no use>	-		
4C	7-6	-	<no use>	-	00~FF	21
	5-0	GAM14[13: 8]	Reverse γ correction 14	Reverse γ coefficient value is set. Input Output value of 192 [LSB]		
4D	7-4	GAM14[7: 4]			00~FF	E0
	3-0	-	<no use>	-		
4E	7-6	-	<no use>	-	00~FF	2F
	5-0	GAM15[13: 8]	Reverse γ correction 15	Reverse γ coefficient value is set. Input Output value of 224 [LSB]		
4F	7-4	GAM15[7: 4]			00~FF	90
	3-0	-	<no use>	-		
50	7	-	<no use>	-	00~FF	40
	6-0	GAM16[14: 8]	Reverse γ correction 16	Reverse γ coefficient Input Output value of 256 [LSB]		
51	7-5	GAM16[7: 5]			00~FF	00
	4-0	-	<no use>	-		

Sub Address	Data bit	Symbol	Item	Function	Setting [hex]	
					RANGE	INITIAL value
E5	7-0	UVrs	USER Vrs	Setting Vrs voltage Standard equation: Vrs=2.99*UVrs/255	00~AA	Adjusted in factory
E6	7-0	UVra	USER Vra	Setting Vra voltage Standard equation: Vra=2.99*UVra/255	00~AA	Adjusted in factory
FE	7-3	—	—	Be sure to use the display with the setting fixed to 0.	0	0
	2	RCLVr	UVrs/UVra RECALL	Resetting the UVrs, UVra in both of register and EEPROM to the initial value by setting RCLVr to 1. This setting automatically returns to 0 after resetting the UVrs,Uvra.	0:Normal 1: UVrs,UVra initialized	0
	1	EWRVr	UVrs/UVra Write	Storing the UVrs,UVra in register to EEPROM by setting EWRVr to 1. This setting automatically returns to 0 after resetting the UVrs,UVra.	0:Normal 1: UVrs,UVra stored in EEPROM	0
	0	—	—	Be sure to use the display with the setting fixed to 0.	0	0
FF	7-1	—	—	Be sure to use the display with the setting fixed to 0.	0	0
	0	DSET	Data setup	When the DSETEN setting is 1, setting this bit causes all the register setups that have been set up to now, to be reflected to the operation status of this product. They are reflected from the next field after this bit is accepted.	0: Normal 1: Execute	0

3.3.2 Function of X-SUS Board

(1) DC/DC power supply block

Vs (+85V) → Vw (+185V) / Vx (+55V)

Vcc (+5V) → XFve (+18V, floating) / Ve (+17V)

(2) X switching block

Switching during address period

Switching during sustain period

Switching during reset period

(3) Current detector block

Isx (sustain) current detection

Iax (address) current detection

(4) Voltage detector block

Vs (sustain) voltage detection

Va (address) voltage detection

3.3.3 Function of Y-SUS Board

(1) DC/DC power supply block

Vcc (+5V) →YFve (+18V, floating) / Ve (+17V)

(2) Switching block

Switching during address period

Switching during sustain period

Switching during reset period

(3) Current detector block

Isy (sustain) current detection

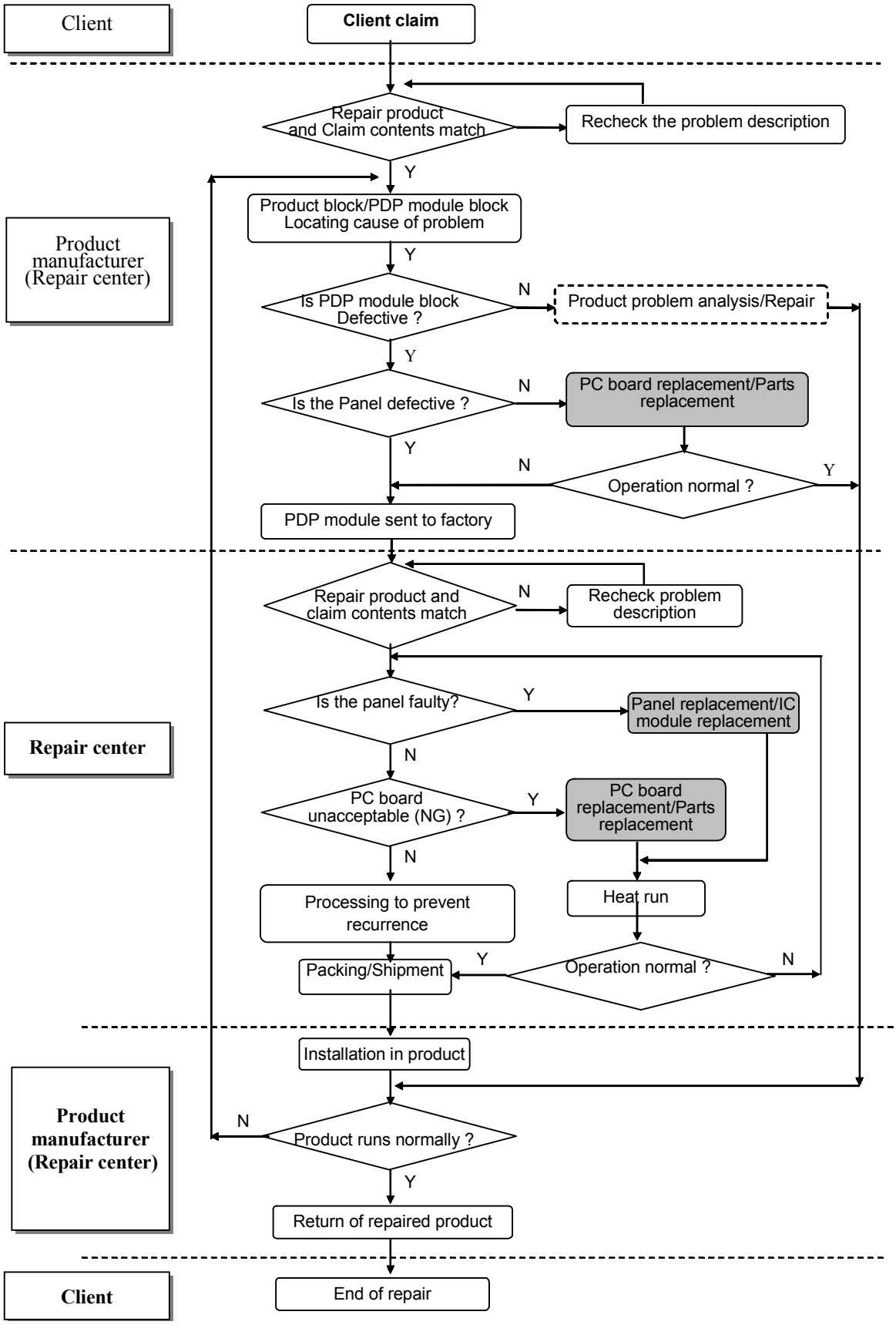
Isp (SDM) current detection

3.4 PROTECTION FUNCTION

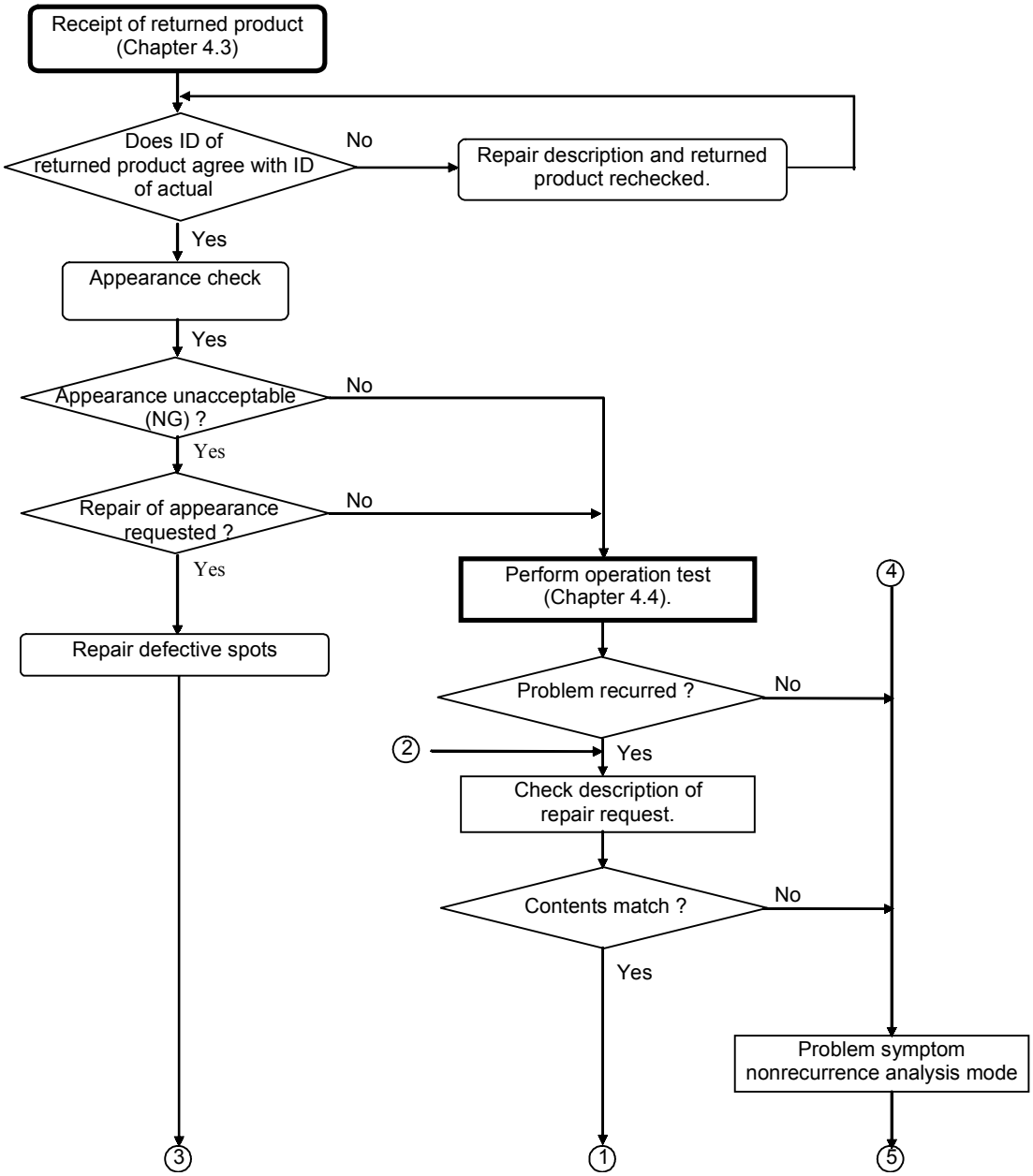
Abnormality part		State of protection operation (√:State change、There is no change at the blank.)										Reactivation condition when abnormal content is excluded	
		State	Vw,	Vx	Vs	Va	Vex	Vey	Vcc	Vpr	Va ux	AC Re-turning on	PFCgo Reset
Vw	Overvoltage	Stop(no latch)	√	√	√	√	√	√	√				
	Overcurrent	Delay Latch	√	√	√	√	√	√	√			Yes	Yes
Vx	Overvoltage	Stop(no latch)	√	√	√	√	√	√	√			Yes	Yes
	Overcurrent	Delay Latch	√	√	√	√	√	√	√			Yes	Yes
Vs	Overvoltage	Latch	√	√	√	√	√	√	√			Yes	Yes
	Low voltage	Latch	√	√	√	√	√	√	√			Yes	Yes
	Overcurrent	Delay Latch	√	√	√	√	√	√	√			Yes	Yes
Va	Overvoltage	Latch	√	√	√	√	√	√	√			Yes	Yes
	Low voltage	Latch	√	√	√	√	√	√	√			Yes	Yes
	Overcurrent	Delay Latch	√	√	√	√	√	√	√			Yes	Yes
Vex Vey	Overvoltage	Stop(no latch)	√	√	√	√	√	√	√			Yes	Yes
	Overcurrent	Voltage pendency(no latch)	√	√	√	√	√	√	√			Yes	Yes
Vcc	Overvoltage	Latch	√	√	√	√	√	√	√			Yes	Yes
	Overcurrent	Delay Latch	√	√	√	√	√	√	√			Yes	Yes
Vpr1	Overvoltage	Latch	√	√	√	√	√	√	√	√	√	Yes	
	Overcurrent	Delay Latch	√	√	√	√	√	√	√	√	√	Yes	
Vpr2	Overcurrent	Delay Latch	√	√	√	√	√	√	√	√	√	Yes	
Vaux	Overvoltage	Latch	√	√	√	√	√	√	√	√	√	Yes	
	Overcurrent (Note 2)	Voltage pendency(no latch)	√	√	√	√	√	√	√				
PSU Heat sink	Temperature	Latch	√	√	√	√	√	√	√	√	√	Yes	

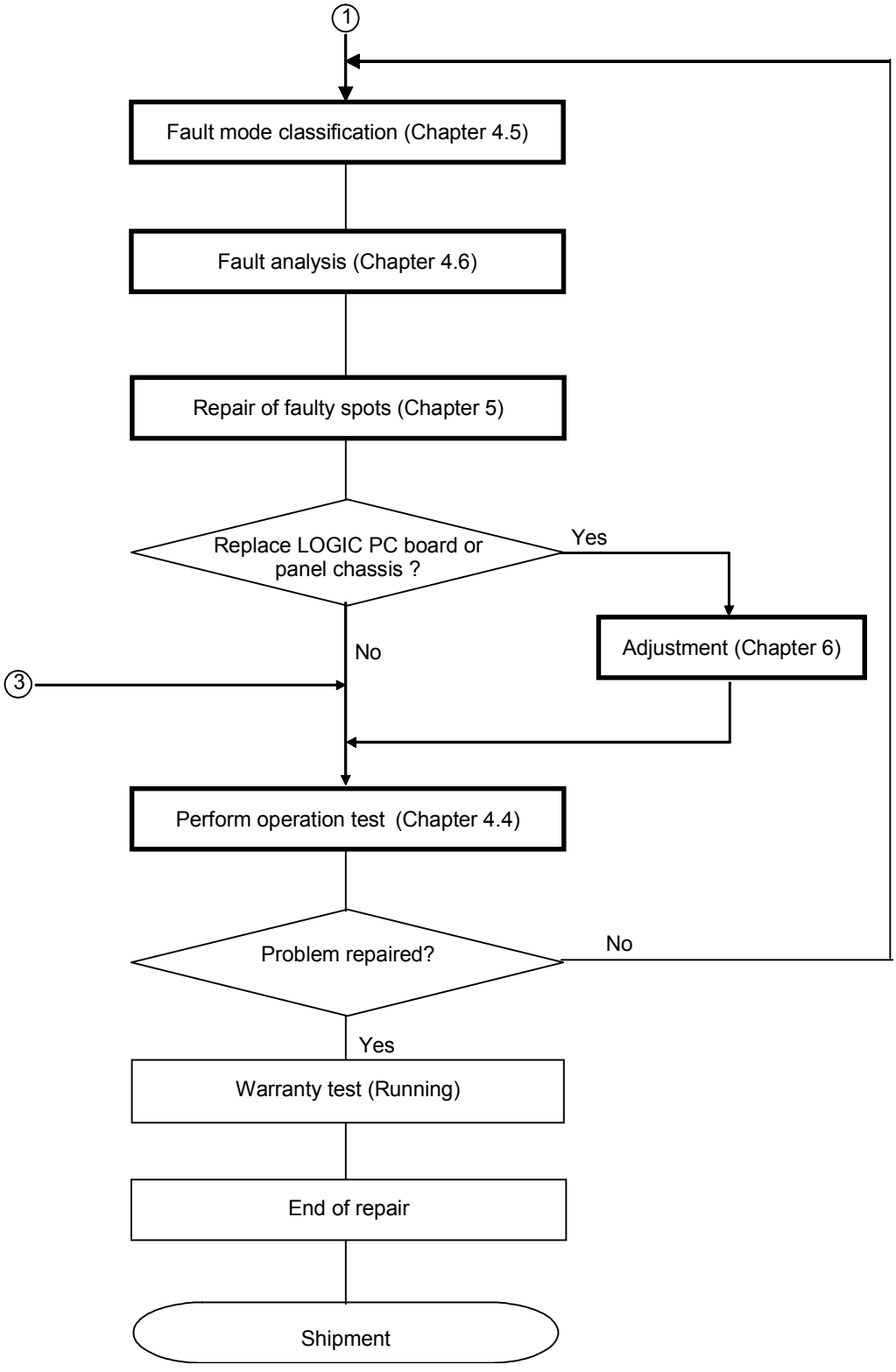
4 PROBLEM ANALYSIS

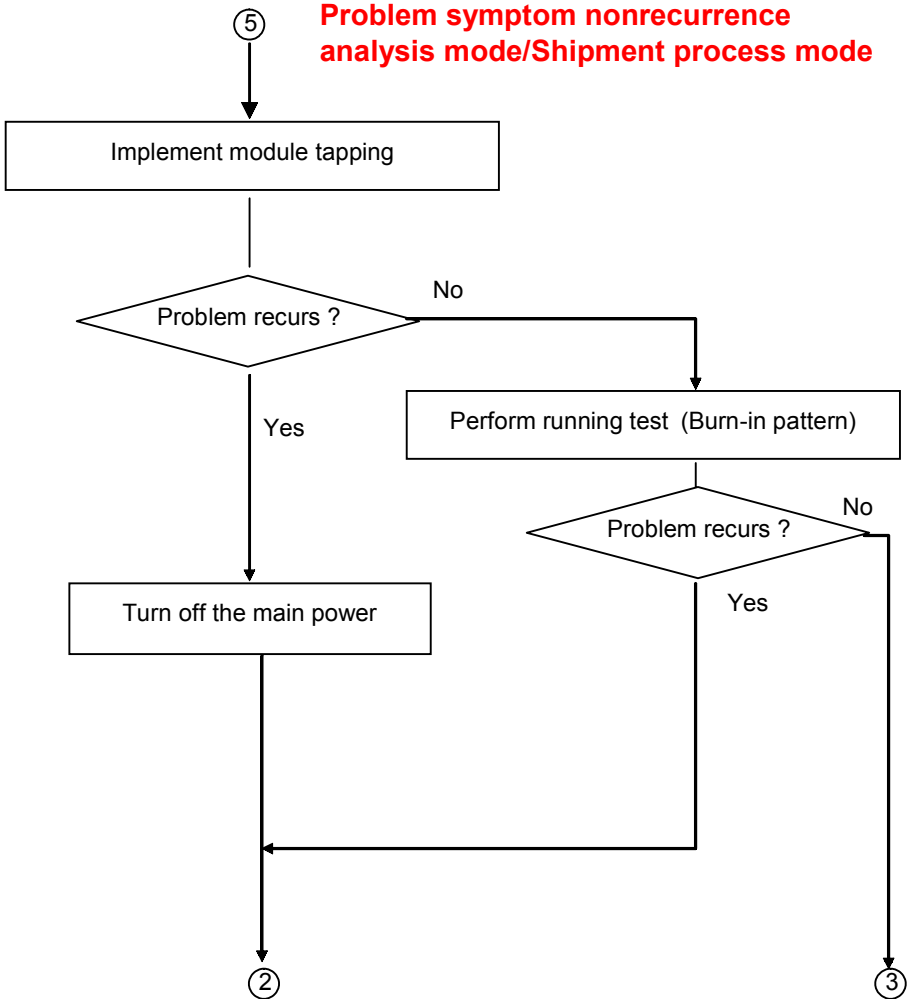
4.1 OUTLINE OF REPAIR FLOW



4.2 OUTLINE OF PDP MODULE REPAIR FLOW




1
Fault mode classification (Chapter 4.5)
Fault analysis (Chapter 4.6)
Repair of faulty spots (Chapter 5)
Replace LOGIC PC board or panel chassis ?
Yes
Adjustment (Chapter 6)
No
3
Perform operation test (Chapter 4.4)
Problem repaired?
No
Yes
Warranty test (Running)
End of repair
Shipment


5
Problem symptom nonrecurrence analysis mode/Shipment process mode
Implement module tapping
Problem recurs ?
No
Yes
Perform running test (Burn-in pattern)
Problem recurs ?
No
Yes
Turn off the main power
2
3

4.3 CHECKING THE PRODUCT REQUESTED FOR REPAIR

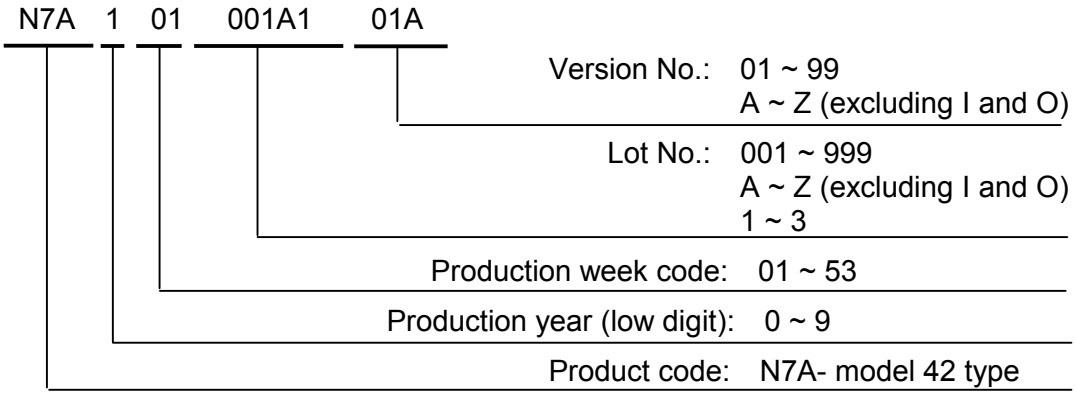
Check the serial ID number of the product requested for repair before starting the problem analysis and repair.

Structure of serial ID number is shown below.

(1) Checking serial ID number of PDP module (14 digits)

The serial ID number of the product that is brought in for service and that of the completed panel chassis has the structure as shown below.

The serial ID number is shown on the bar code label that is attached to the rear of the chassis (aluminum).



Module product label

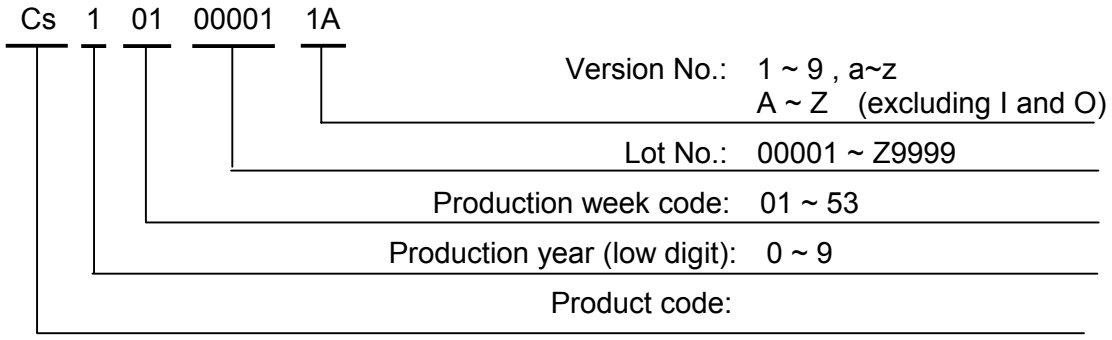
Serial ID label of panel chassis

*** The module serial ID number and the serial ID number of the completed chassis (product requested for repair) are usually the same when the product is brought in for repair for the first time.**

(2) Checking serial ID number of constituent PC boards (12 digits)

The serial ID number of the module constituent PC boards has the following structure.

The serial ID number is shown on the bar code label that is attached to each PC board.



4.4 OPERATION TEST PROCEDURE

(1) Prepare the test equipment and the module requested for repair.

(2) Affix to the stand (jig) the module requested for repair.

(3) Connect LOGIC board connector CN1 of the module to the Interface board (jig)CN5 with the dedicated signal cable.

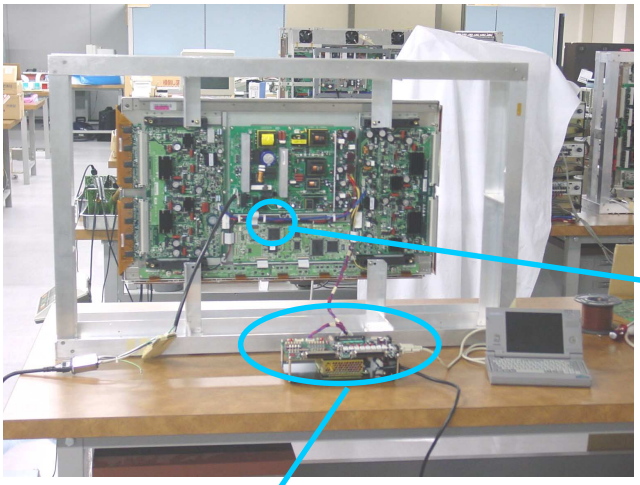
(4) Connect the AC power cable to CN61 on the PSU board of the module requested for repair.

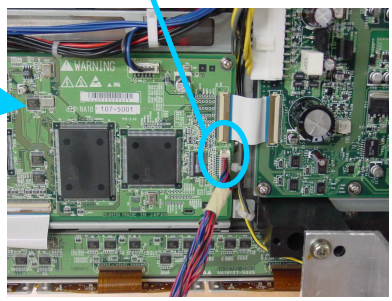
(5) Turn on the AC power to the interface board (jig).

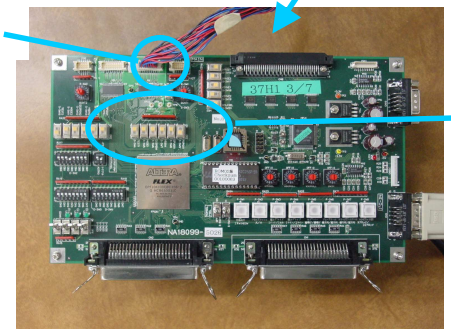
(6) Select the signal used when a problem occurs, or an all white pattern.

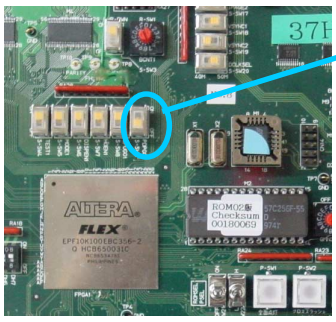
(7) Set the PDP go switch on the Interface board (jig) to ON.
(The main power of the module is turned on.)

Check Fault Symptom

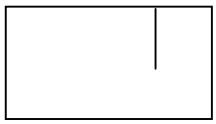
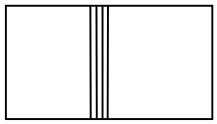
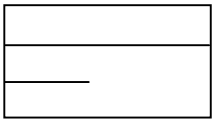
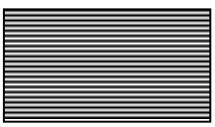


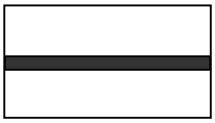
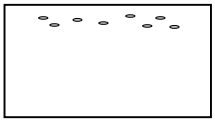






4.5 FAULT SYMPTOM

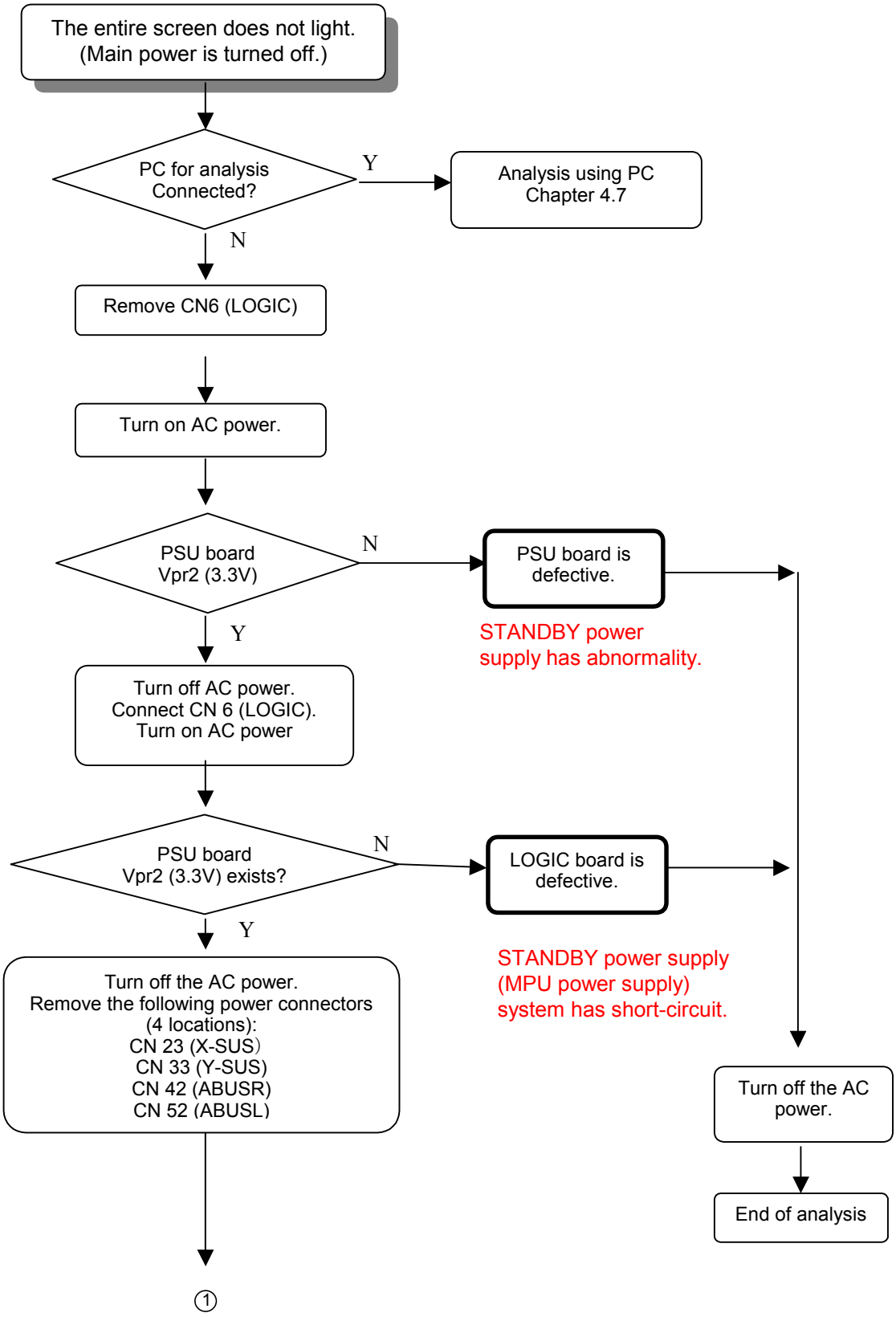
NO	Fault contents	Fault status		Suspected fault location	Analysis procedure and measure
1	Entire screen does not light.	After momentarily going on, the screen becomes black immediately or after a few seconds. (Main power is turned off.)		X-SUS Y-SUS PSU Panel chassis LOGIC ABUSL ABUSR	Refer to Chapter 4.6.1
2		Screen lights dimly even on the back screen.		LOGIC	Replace LOGIC board
3	Vertical line	Single vertical line (of different color)		Panel chassis LOGIC	Refer to Chapter 4.6.2
4		Vertical line from the middle of effective scan area (Vertical line of different color)		Panel chassis	Replace panel chassis
5	Vertical bar	Bar width of 1/7 of horizontal size or in multiples of 1/7, is displayed. Abnormal display.		Panel chassis ABUSL ABUSR LOGIC Above boards are connected.	Refer to Chapter 4.6.2
6		Bar width of 3/7 or 4/7 of the screen width, is displayed. Abnormal display. (Vertical line of different color)		ABUSL ABUSR LOGIC Above boards are connected.	Refer to Chapter 4.6.2
7	Horizontal line	Single horizontal line (No light) or single horizontal line does not light among the effective scanning area. Single horizontal line does not light.		Panel chassis	Replace panel chassis
8		Every other line(No light) Entire screen		X-SUS Y-SUS	Replace X-SUS Y-SUS Board

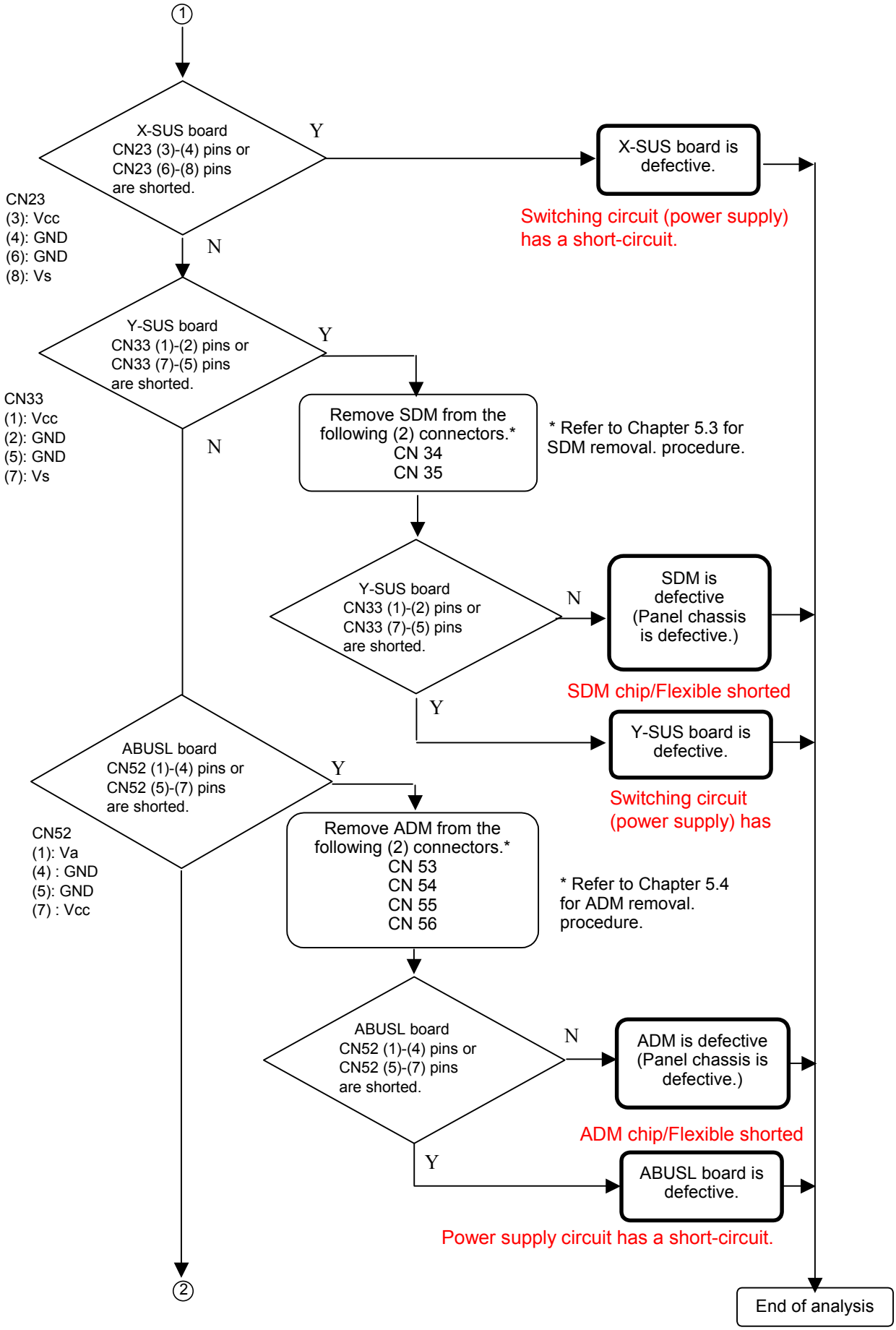
NO	Fault contents	Fault status		Suspected fault location	Analysis procedure and measure
9	Horizontal bar	Bar width of 1/8 or multiples of 1/8 of the screen height, is displayed. Abnormal (Screen does not light)		Panel chassis	Replace panel chassis
10		Bar width of 1/2 of the screen height. Abnormal display (Screen does not light)		Panel chassis Y-SUS X-SUS Above boards are connected.	Refer to Chapter 4.6.3
11	Image sticking	Fixed display contents are always displayed.		Panel chassis	Perform all white heat run. After judgment, replace panel chassis
12	Stains	Oval-shaped points having abnormal luminance are scattered in the upper or lower part of screen.		Panel chassis	Perform all white heat run. After judgment, replace panel chassis
13	Twinkle	The entire screen momentarily becomes brighter or darker.			
14	Flicker	The entire screen flickers continuously.		Poor connector contact (CN2,3,21,31)	Connector / cable re-connection or Cable exchange
15	Luminance is abnormal	Screen is too dark or too bright. (Out of specifications)			
16	Chrominance is abnormal	Colors cannot be displayed correctly.		LOGIC	Replace LOGIC board
17	Sync is disturbed			LOGIC	Replace LOGIC board
18	Picture distorted			LOGIC	Replace LOGIC board
19	Steps of gradation are skipped	Luminance linearity is poor.		LOGIC	Replace LOGIC board
20	Abnormal sound			PSU X-SUS Y-SUS (Core is broken, or transformer is abnormal.)	Locate cause of abnormality from listening and viewing. Replace the cause of problem.

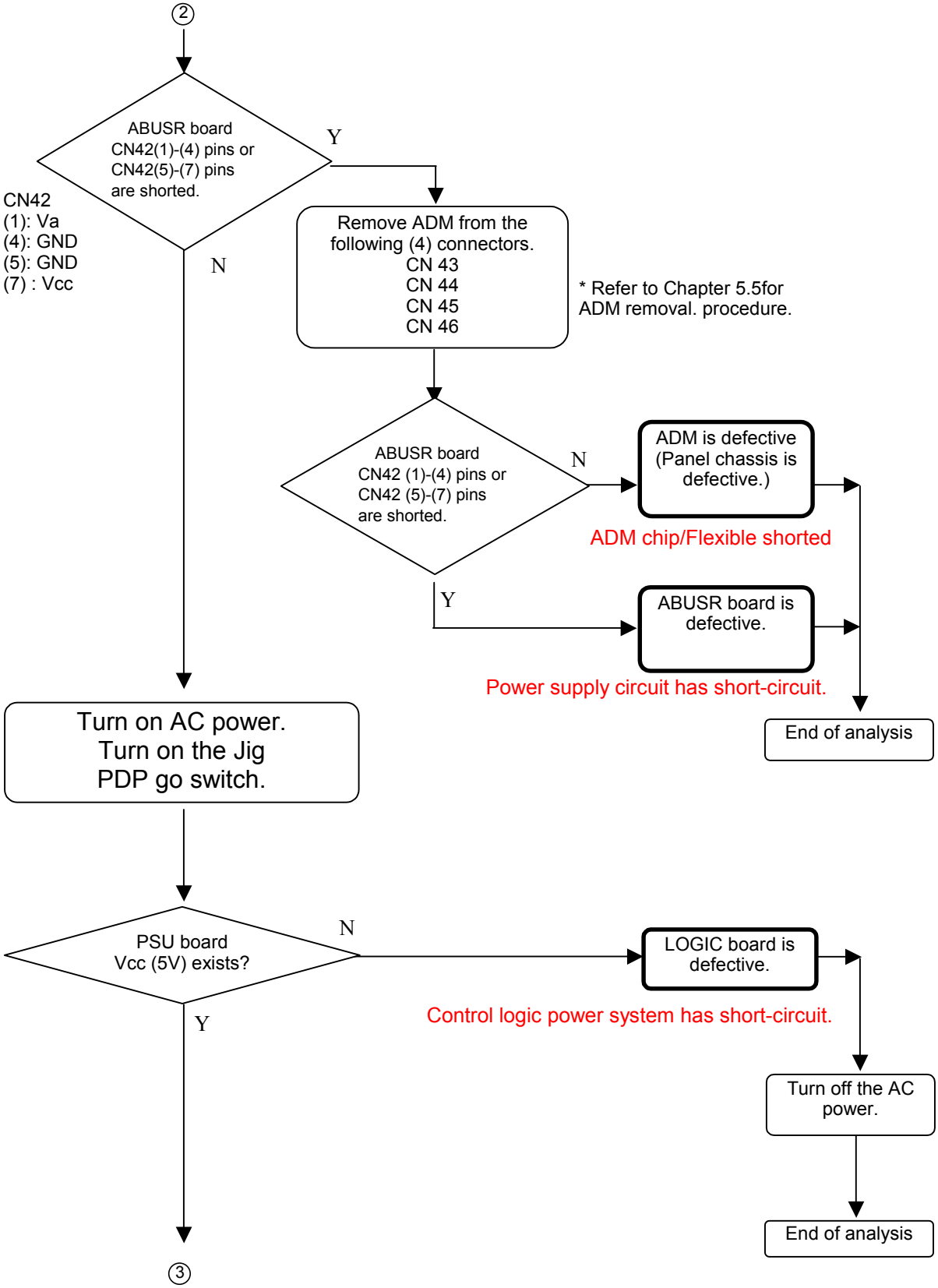
NO	Fault contents	Fault status		Suspected fault location	Analysis procedure and measure
21	Control on external communication is abnormal	Contrast, color temperature adjustment and ϒ cannot be changed.		LOGIC	Replace LOGIC board

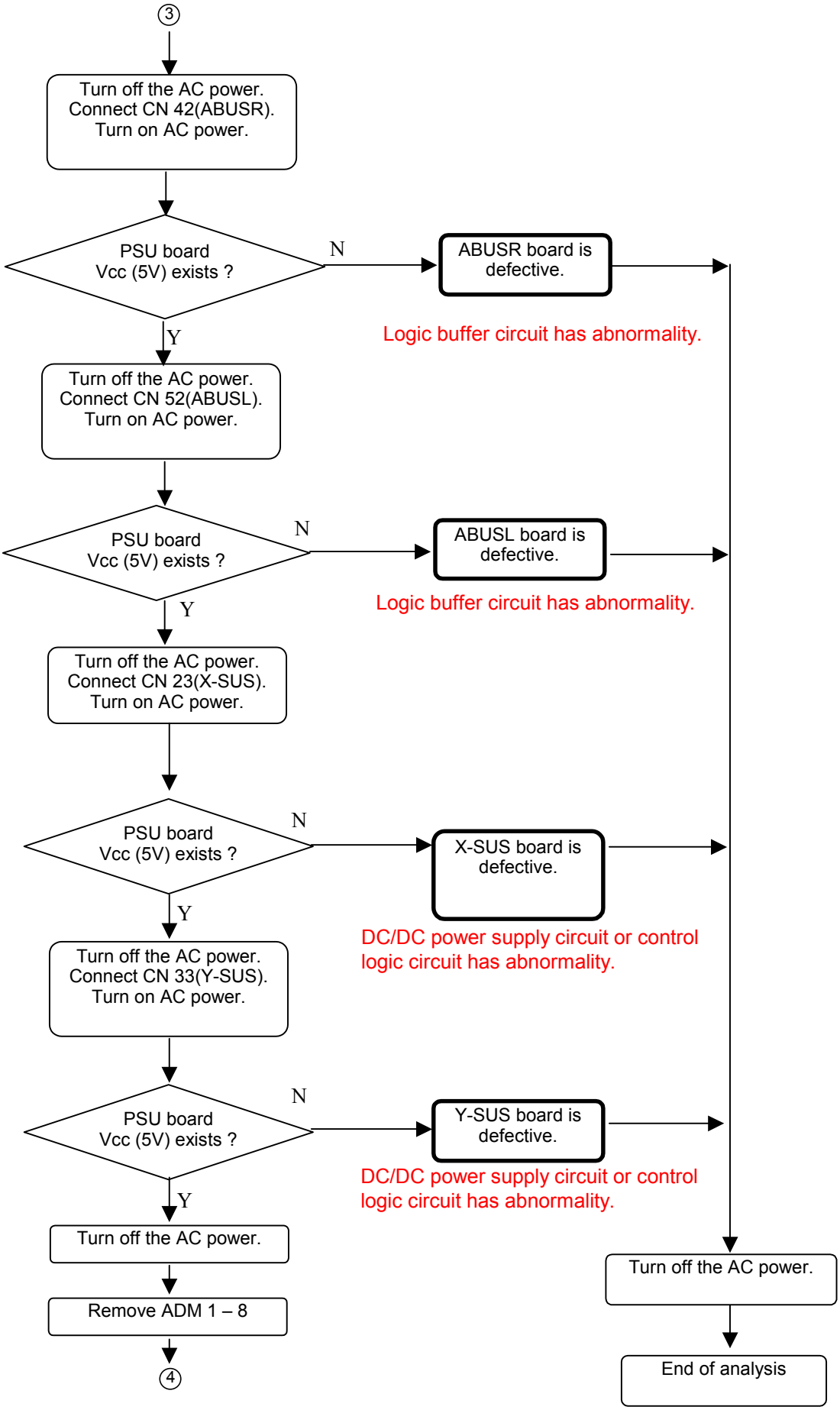
4.6 PROBLEM ANALYSIS PROCEDURE

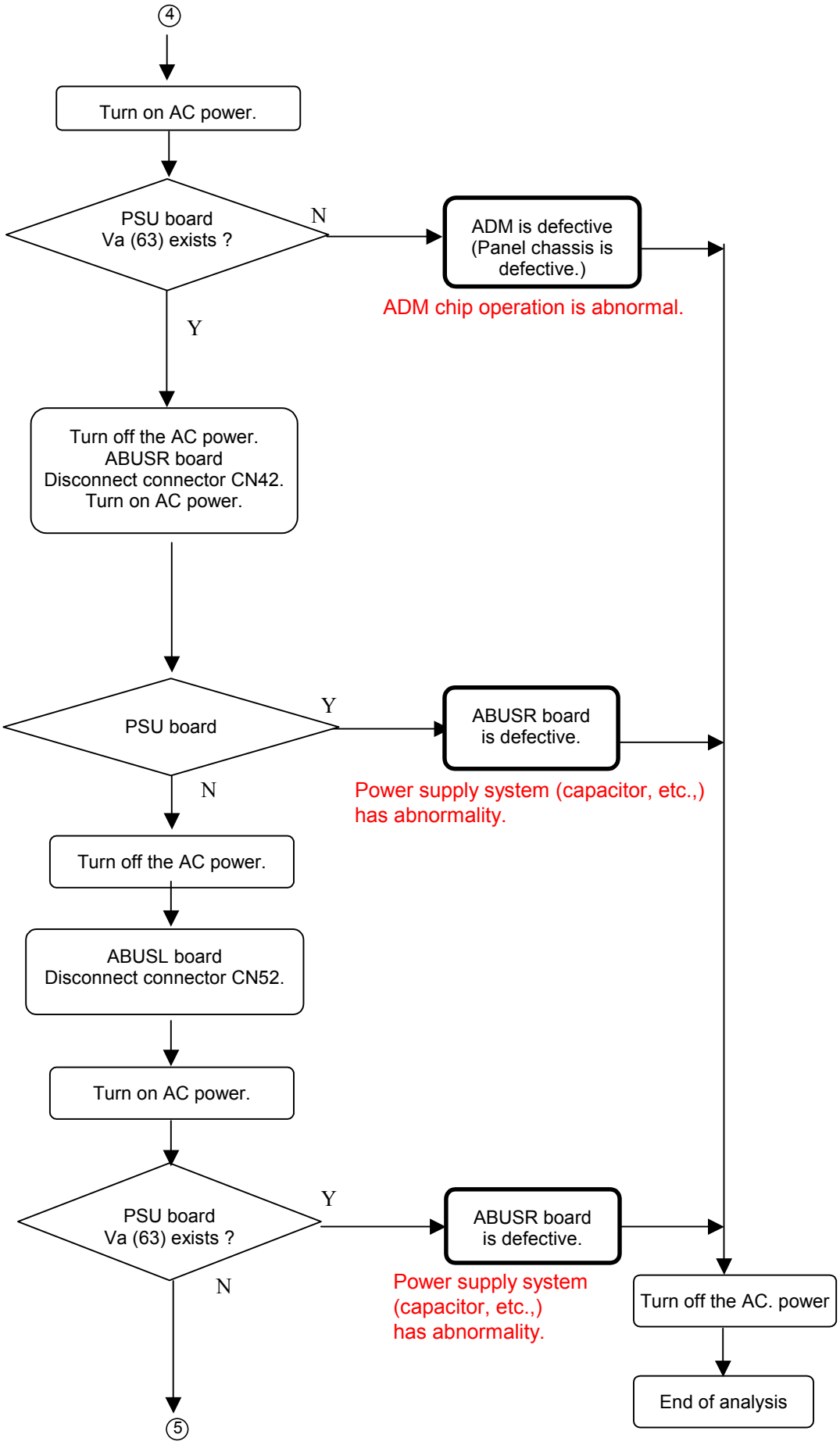
4.6.1 "The entire screen does not light.(Main power is turned off)" Problem analysis procedure

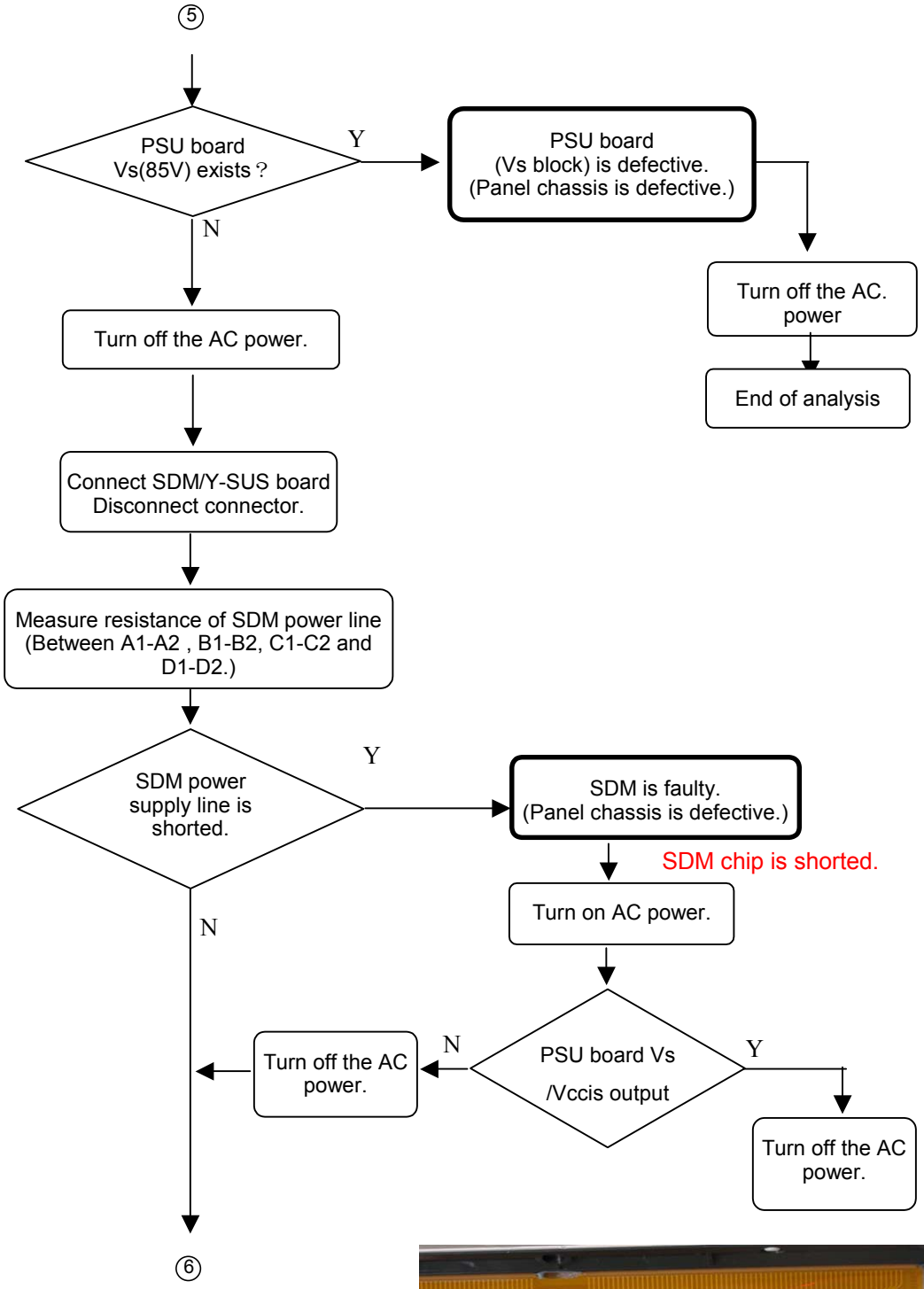


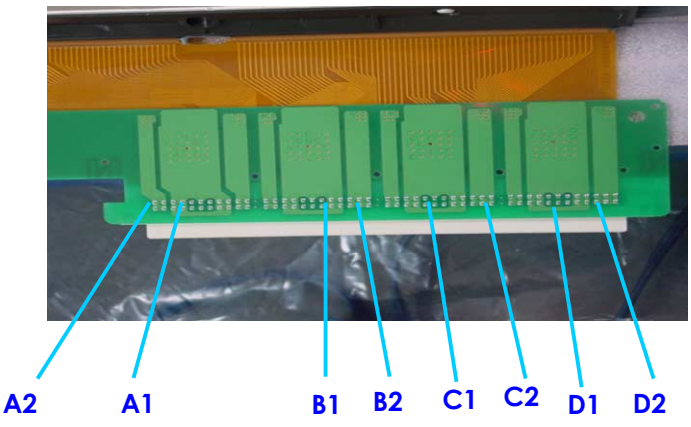

①
X-SUS board
CN23 (3)-(4) pins or
CN23 (6)-(8) pins
are shorted.
Y
X-SUS board is
defective.
Switching circuit (power supply)
has a short-circuit.
CN23
(3): Vcc
(4): GND
(6): GND
(8): Vs
N
Y-SUS board
CN33 (1)-(2) pins or
CN33 (7)-(5) pins
are shorted.
Y
CN33
(1): Vcc
(2): GND
(5): GND
(7): Vs
N
Remove SDM from the
following (2) connectors.*
CN 34
CN 35
* Refer to Chapter 5.3 for
SDM removal. procedure.
Y-SUS board
CN33 (1)-(2) pins or
CN33 (7)-(5) pins
are shorted.
N
SDM is
defective
(Panel chassis
is defective.)
SDM chip/Flexible shorted
Y
Y-SUS board is
defective.
Switching circuit
(power supply) has
ABUSL board
CN52 (1)-(4) pins or
CN52 (5)-(7) pins
are shorted.
Y
CN52
(1): Va
(4) : GND
(5): GND
(7) : Vcc
Remove ADM from the
following (2) connectors.*
CN 53
CN 54
CN 55
CN 56
* Refer to Chapter 5.4
for ADM removal.
procedure.
ABUSL board
CN52 (1)-(4) pins or
CN52 (5)-(7) pins
are shorted.
N
ADM is defective
(Panel chassis is
defective.)
ADM chip/Flexible shorted
Y
ABUSL board is
defective.
Power supply circuit has a short-circuit.
②
End of analysis

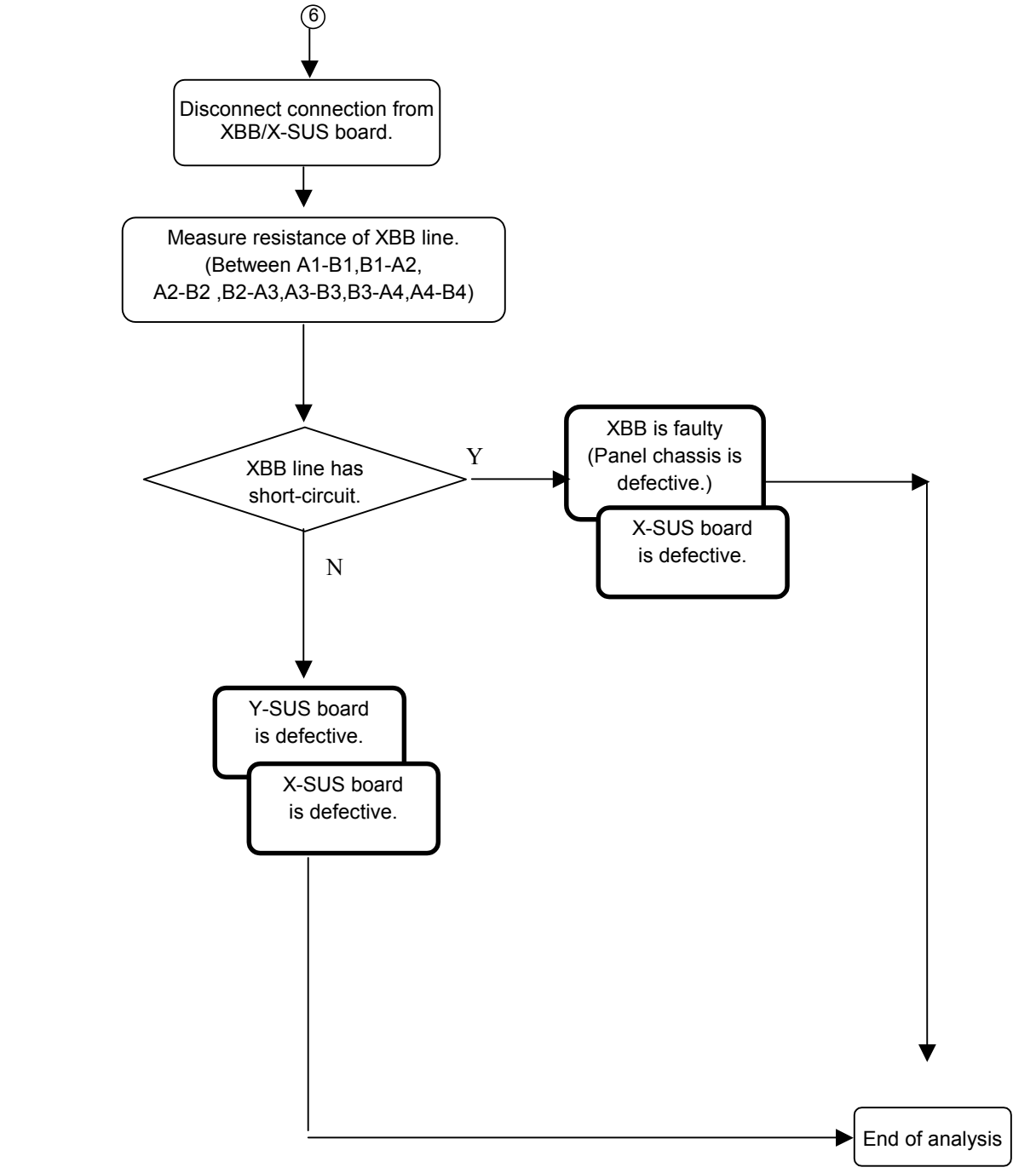

②
ABUSR board
CN42(1)-(4) pins or
CN42(5)-(7) pins
are shorted.
Y
N
CN42
(1): Va
(4): GND
(5): GND
(7) : Vcc
Remove ADM from the
following (4) connectors.
CN 43
CN 44
CN 45
CN 46
* Refer to Chapter 5.5for
ADM removal. procedure.
ABUSR board
CN42 (1)-(4) pins or
CN42 (5)-(7) pins
are shorted.
N
ADM is defective
(Panel chassis is
defective.)
ADM chip/Flexible shorted
Y
ABUSR board is
defective.
Power supply circuit has short-circuit.
End of analysis
Turn on AC power.
Turn on the Jig
PDP go switch.
PSU board
Vcc (5V) exists?
N
LOGIC board is
defective.
Control logic power system has short-circuit.
Y
Turn off the AC
power.
End of analysis
③

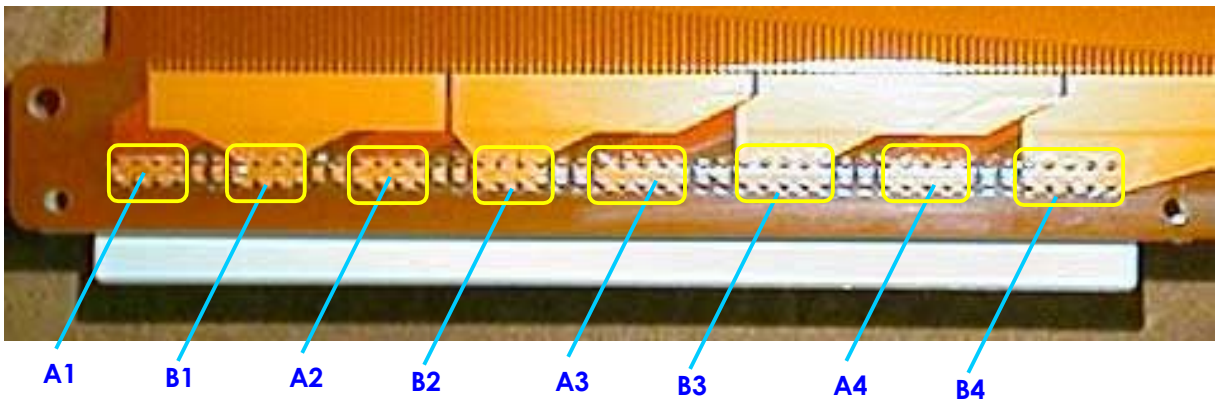

③
Turn off the AC power.
Connect CN 42(ABUSR).
Turn on AC power.
PSU board
Vcc (5V) exists ?
N
ABUSR board is
defective.
Logic buffer circuit has abnormality.
Y
Turn off the AC power.
Connect CN 52(ABUSL).
Turn on AC power.
PSU board
Vcc (5V) exists ?
N
ABUSL board is
defective.
Logic buffer circuit has abnormality.
Y
Turn off the AC power.
Connect CN 23(X-SUS).
Turn on AC power.
PSU board
Vcc (5V) exists ?
N
X-SUS board is
defective.
DC/DC power supply circuit or control
logic circuit has abnormality.
Y
Turn off the AC power.
Connect CN 33(Y-SUS).
Turn on AC power.
PSU board
Vcc (5V) exists ?
N
Y-SUS board is
defective.
DC/DC power supply circuit or control
logic circuit has abnormality.
Y
Turn off the AC power.
Remove ADM 1 – 8
④
Turn off the AC power.
End of analysis


④
Turn on AC power.
PSU board
Va (63) exists ?
N
ADM is defective
(Panel chassis is
defective.)
ADM chip operation is abnormal.
Y
Turn off the AC power.
ABUSR board
Disconnect connector CN42.
Turn on AC power.
PSU board
Y
ABUSR board
is defective.
Power supply system (capacitor, etc.,)
has abnormality.
N
Turn off the AC power.
ABUSL board
Disconnect connector CN52.
Turn on AC power.
PSU board
Va (63) exists ?
Y
ABUSR board
is defective.
Power supply system
(capacitor, etc.,)
has abnormality.
N
Turn off the AC. power
End of analysis
⑤

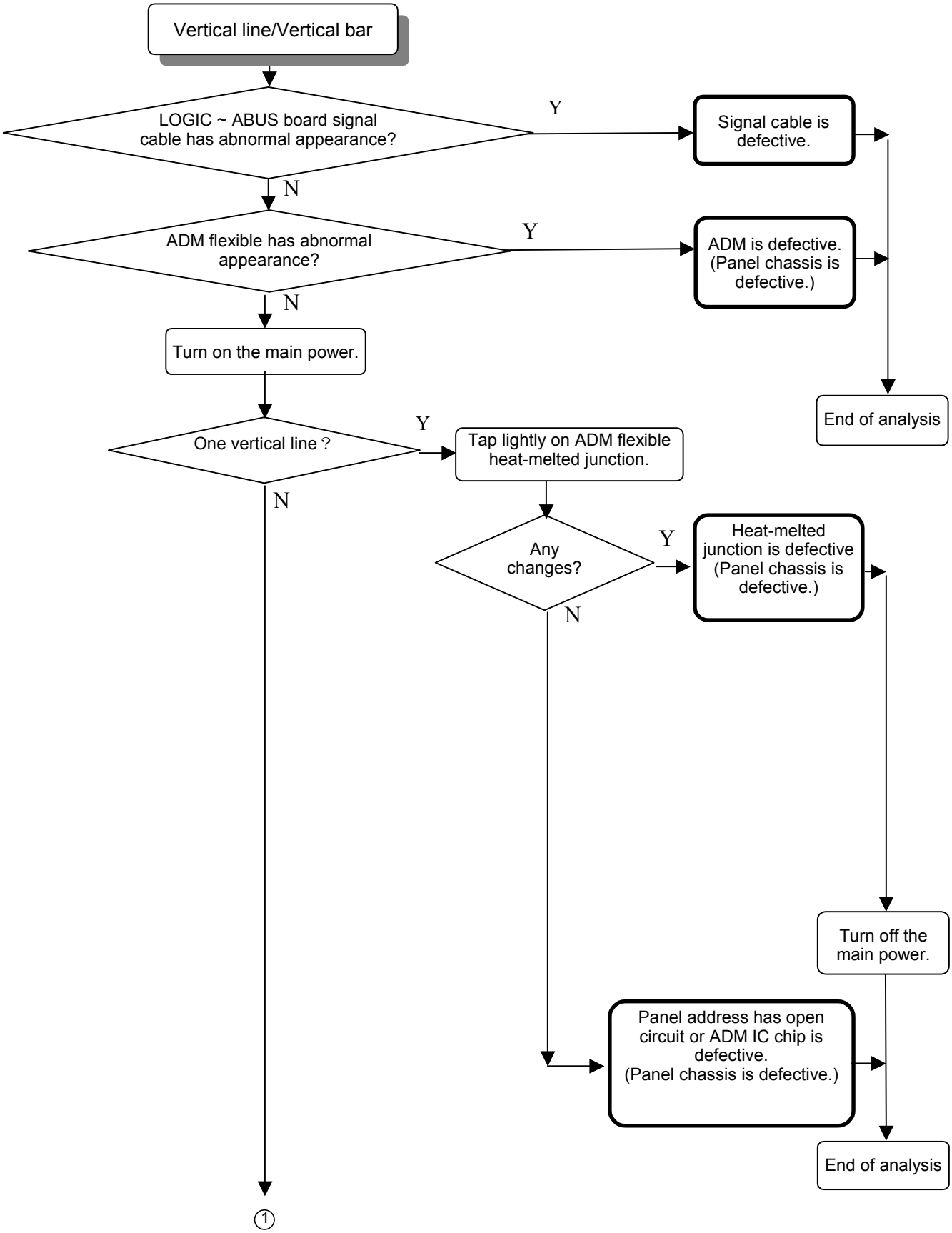

⑤
PSU board
Vs(85V) exists ?
Y
N
PSU board
(Vs block) is defective.
(Panel chassis is defective.)
Turn off the AC.
power
End of analysis
Turn off the AC power.
Connect SDM/Y-SUS board
Disconnect connector.
Measure resistance of SDM power line
(Between A1-A2 , B1-B2, C1-C2 and
D1-D2.)
SDM power
supply line is
shorted.
Y
N
SDM is faulty.
(Panel chassis is defective.)
SDM chip is shorted.
Turn on AC power.
PSU board Vs
/Vccis output
N
Y
Turn off the AC
power.
Turn off the AC
power.
⑥

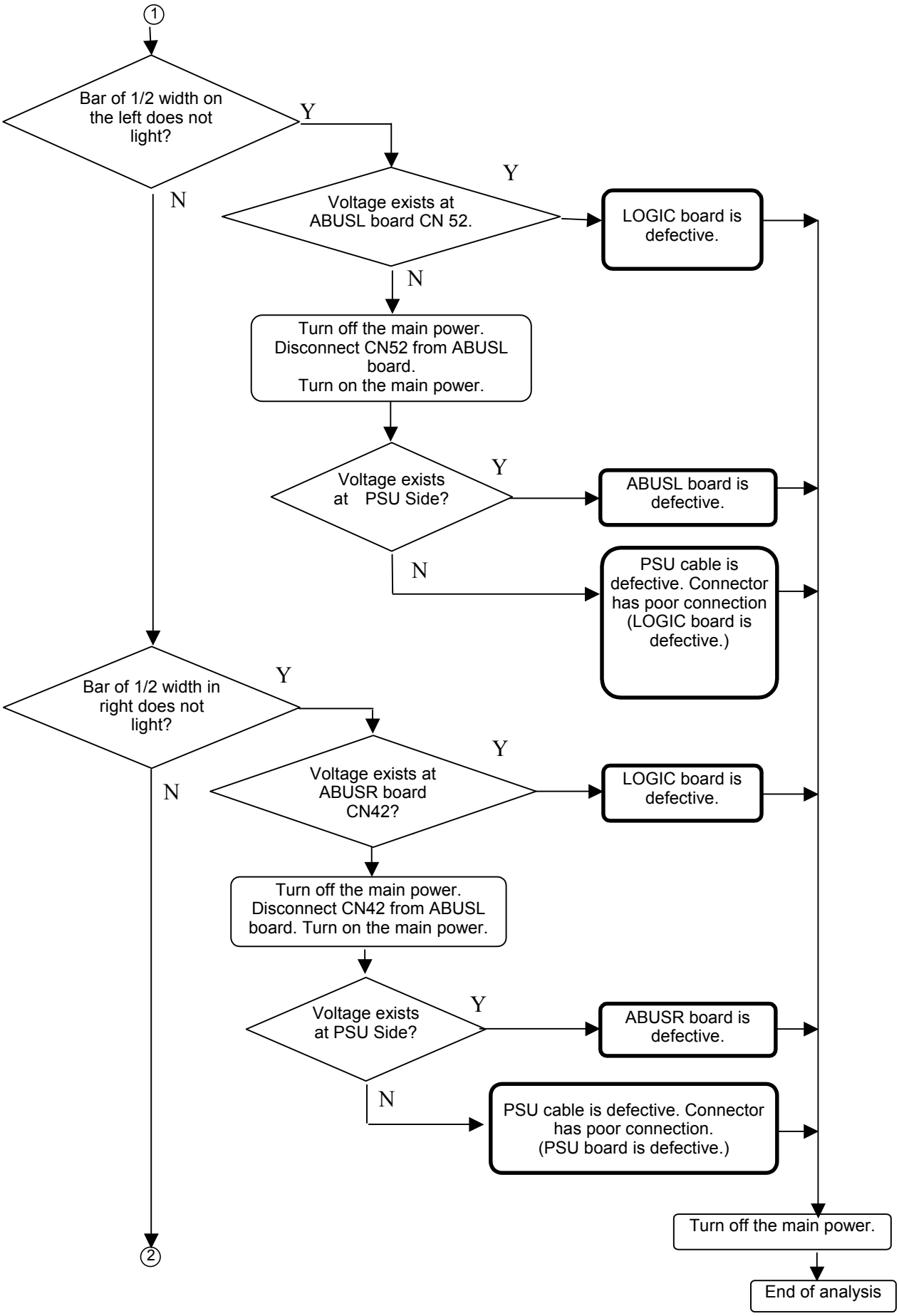

A2
A1
B1
B2
C1
C2
D1
D2

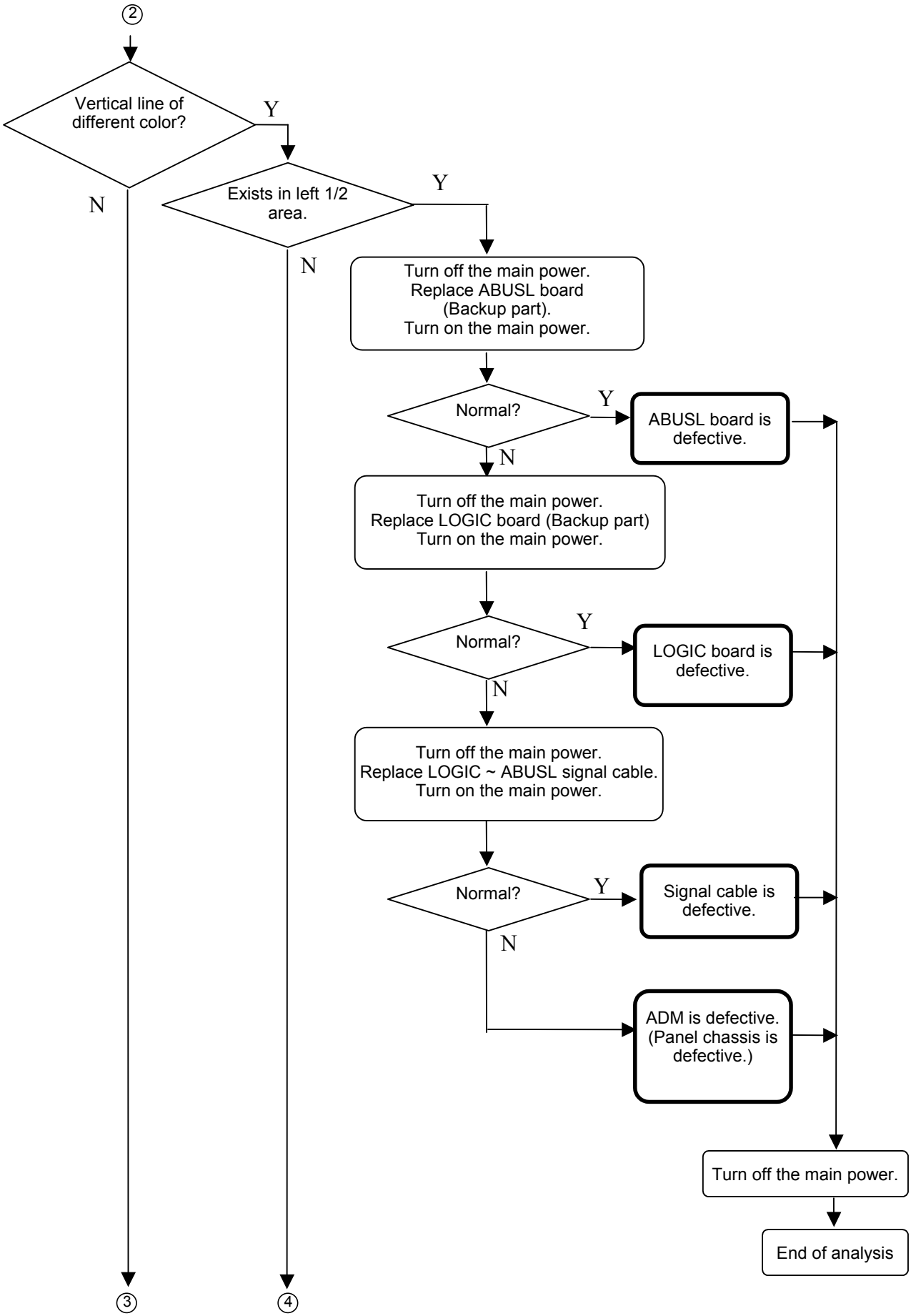

6
Disconnect connection from XBB/X-SUS board.
Measure resistance of XBB line. (Between A1-B1,B1-A2, A2-B2 ,B2-A3,A3-B3,B3-A4,A4-B4)
XBB line has short-circuit.
Y
XBB is faulty (Panel chassis is defective.)
X-SUS board is defective.
N
Y-SUS board is defective.
X-SUS board is defective.
End of analysis

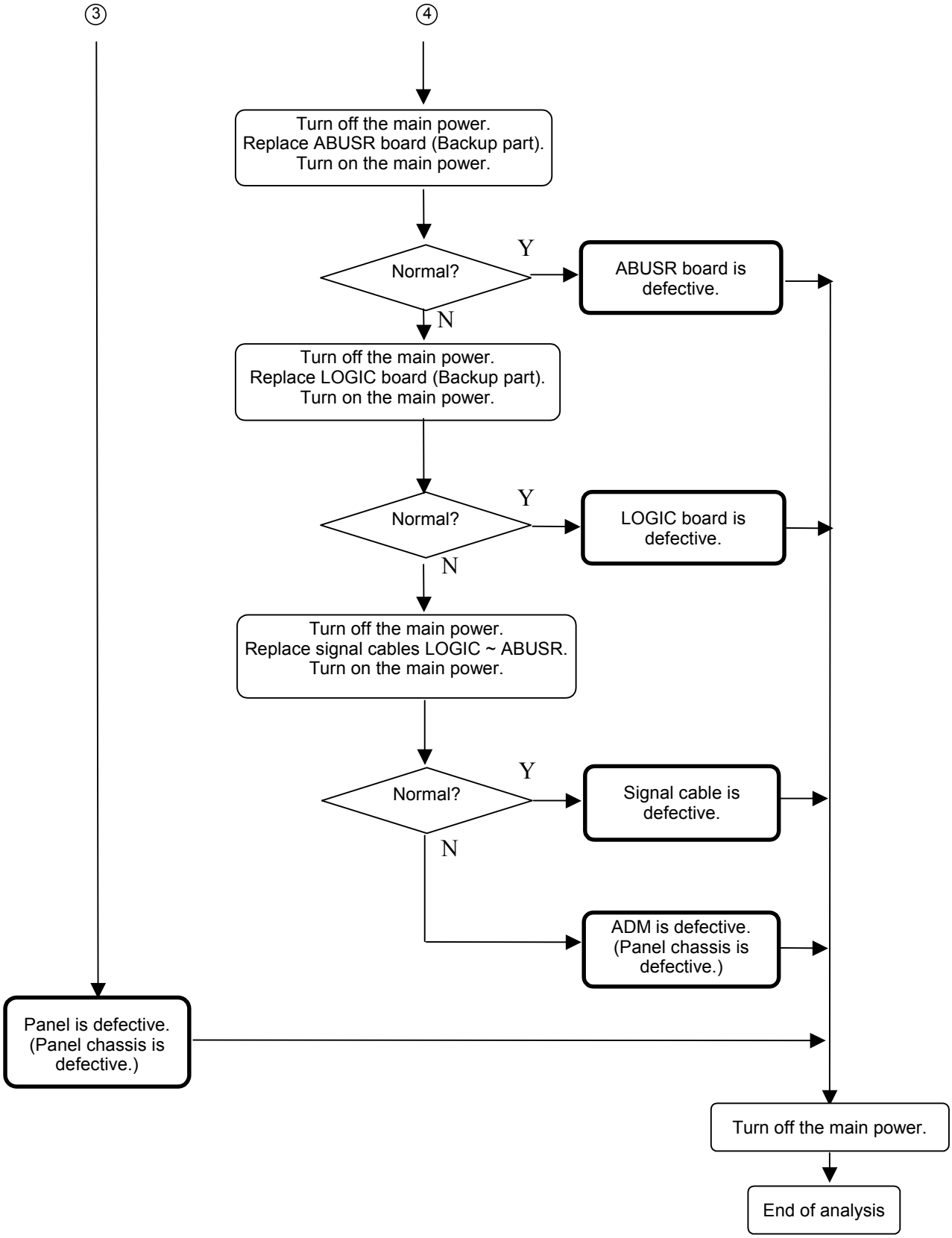

A1
B1
A2
B2
A3
B3
A4
B4

4.6.2 "Vertical line/Vertical bar" Problem analysis procedure

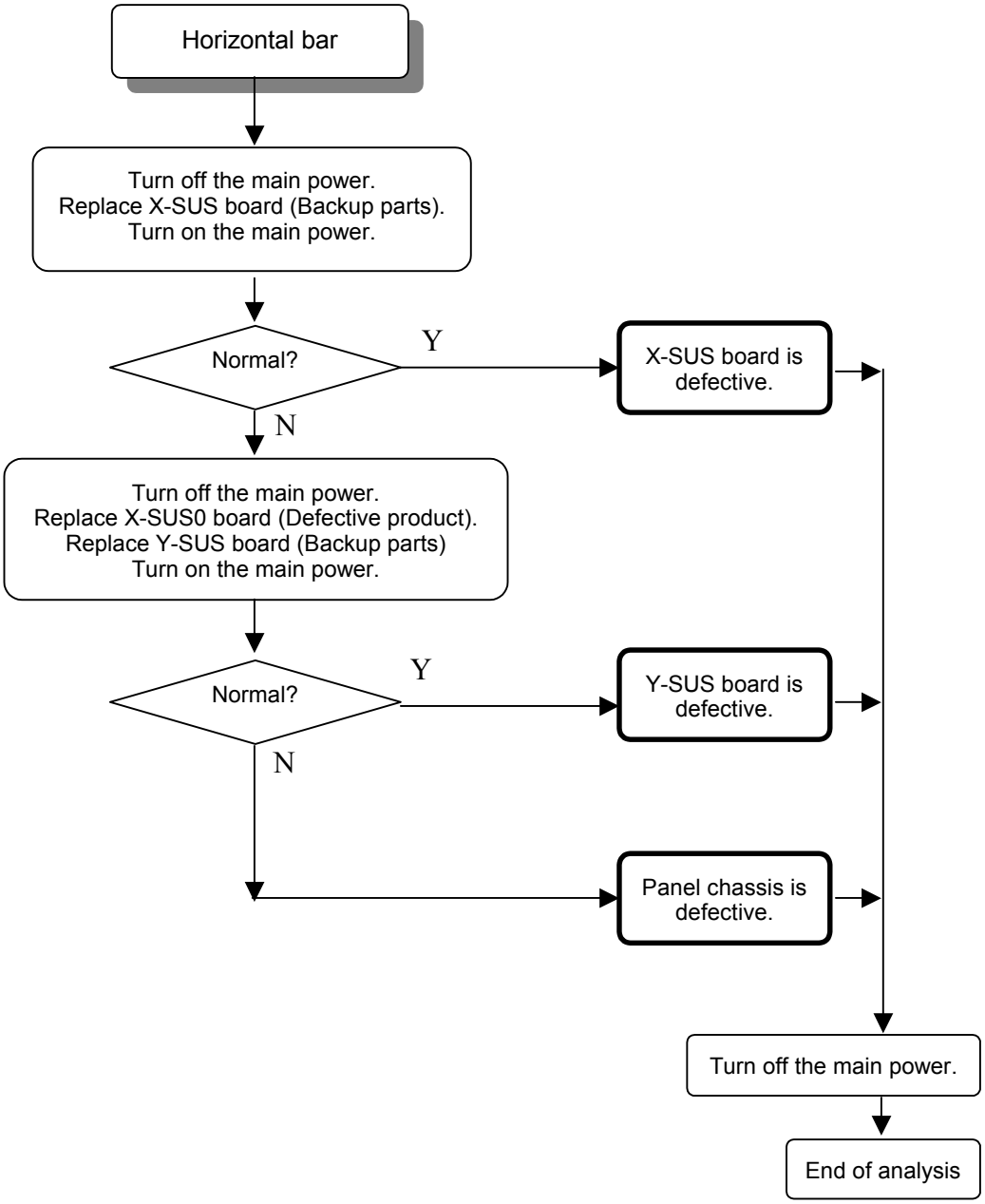



1
Bar of 1/2 width on the left does not light?
Y
N
Voltage exists at ABUSL board CN 52.
Y
LOGIC board is defective.
N
Turn off the main power. Disconnect CN52 from ABUSL board. Turn on the main power.
Voltage exists at PSU Side?
Y
ABUSL board is defective.
N
PSU cable is defective. Connector has poor connection (LOGIC board is defective.)
Bar of 1/2 width in right does not light?
Y
N
Voltage exists at ABUSR board CN42?
Y
LOGIC board is defective.
Turn off the main power. Disconnect CN42 from ABUSL board. Turn on the main power.
Voltage exists at PSU Side?
Y
ABUSR board is defective.
N
PSU cable is defective. Connector has poor connection. (PSU board is defective.)
Turn off the main power.
End of analysis
2


②
Vertical line of different color?
Y
N
Exists in left 1/2 area.
Y
N
Turn off the main power.
Replace ABUSL board
(Backup part).
Turn on the main power.
Normal?
Y
ABUSL board is defective.
N
Turn off the main power.
Replace LOGIC board (Backup part)
Turn on the main power.
Normal?
Y
LOGIC board is defective.
N
Turn off the main power.
Replace LOGIC ~ ABUSL signal cable.
Turn on the main power.
Normal?
Y
Signal cable is defective.
N
ADM is defective.
(Panel chassis is defective.)
Turn off the main power.
End of analysis
③
④


③
④
Turn off the main power.
Replace ABUSR board (Backup part).
Turn on the main power.
Normal?
Y
ABUSR board is defective.
N
Turn off the main power.
Replace LOGIC board (Backup part).
Turn on the main power.
Normal?
Y
LOGIC board is defective.
N
Turn off the main power.
Replace signal cables LOGIC ~ ABUSR.
Turn on the main power.
Normal?
Y
Signal cable is defective.
N
ADM is defective.
(Panel chassis is defective.)
Panel is defective.
(Panel chassis is defective.)
Turn off the main power.
End of analysis

4.6.3 "Horizontal bar" Problem analysis procedure



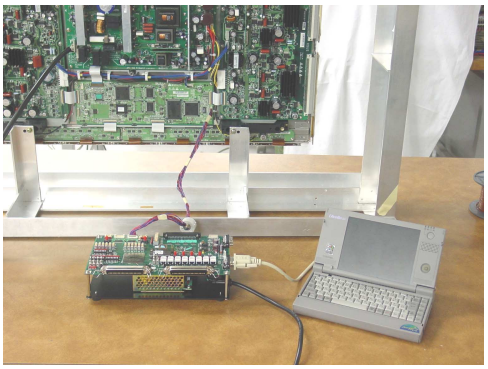
4.7 PROBLEM ANALYSIS USING A PERSONAL COMPUTER

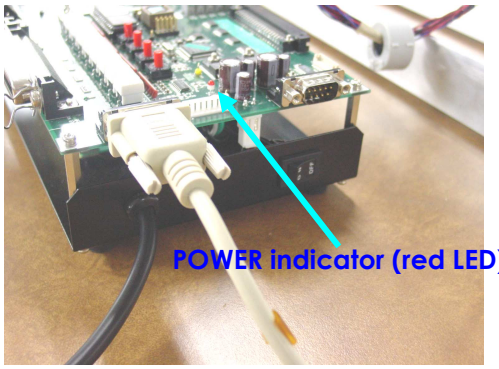
4.7.1 Connecting a computer

(1) Set the module in accordance with Chapter 4.4.

(2) Connect the RS-232C terminal of the computer to the RS-232C terminal of the interface board.

(3) Turn on the main power to the interface board. (Red LED goes on.)





4.7.2 Preparing a computer

(1) Turn on the main power to the computer.

(2) Set the PDPgo switch on the interface board to ON and turn on the main power to the module.

(3) For computer running MS-DOS:

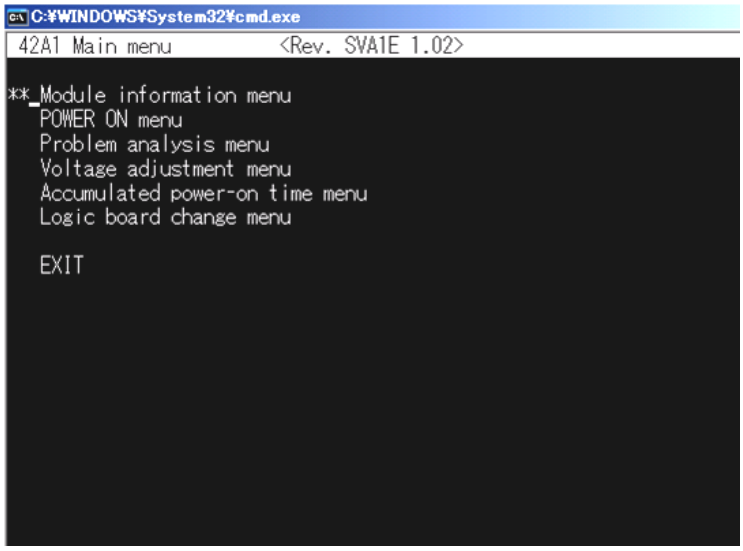
C : \ >FHPA1<ENTER>

For computer running WINDOWS:

Start menu → Run → **FHPA1<ENTER>**

***1: Use COM1: for the computer's communication port.**
***2: Set the communication setup as follows.**
Speed: 9600 bps
Data: 7 bits
Parity: none
Stop bit: 1 bit
In Windows, restart the computer after setting the communication setup.

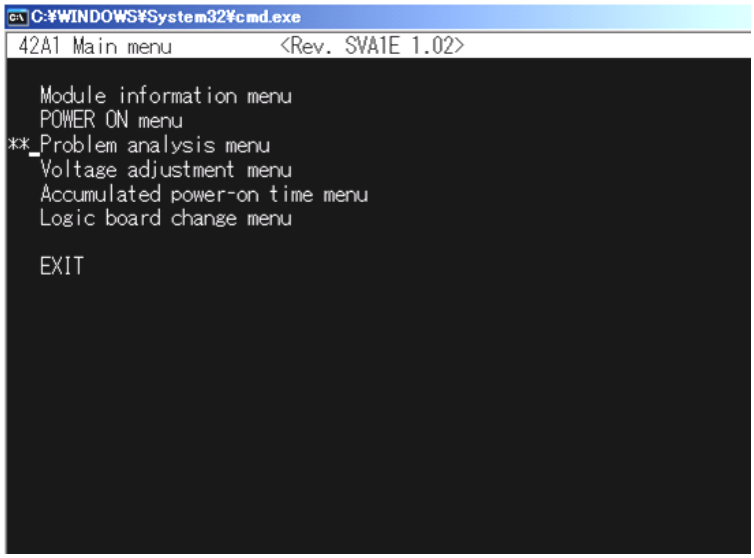
(4) The following menu screen appears.



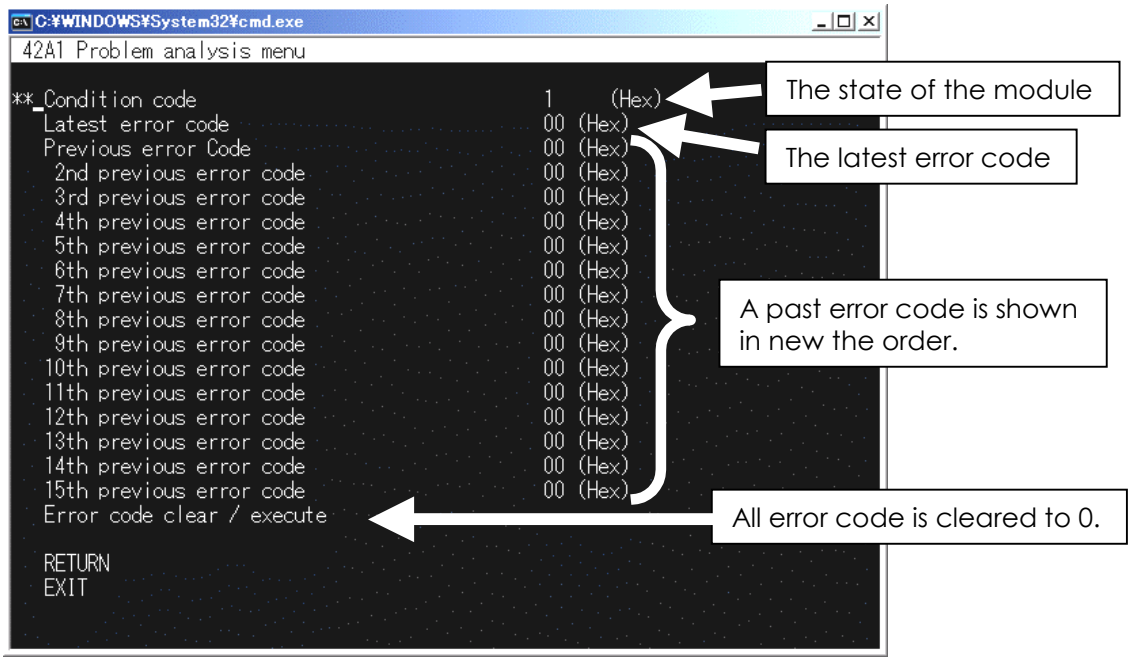
***3: If the program starts up while the module standby power is not yet turned on, the menu screen will not be displayed.**

4.7.3 Problem Analysis Procedure

(1) Select the problem analysis menu from the main menu using the ↑key or ↓key and press <ENTER> key to start the program.



(2) Check the error code (hexadecimal number) from the Latest error code read-out menu and locate the faulty position from the following table.



Example of displaying breakdown analysis

(3) Select RETURN using the ↑key or ↓key and press <ENTER> key to start the program, then the screen returns to the menu screen.

* When EXIT is selected, the screen returns to the WINDOWS or DOS screen.

Error code table

ERR code	Detect position (board)	Contents	Suspected faulty board (In the order of higher probability of defect)							Remarks
			(1)	(2)	(3)	(4)	(5)	(6)	(7)	
00	LOGIC	STANDBY power is stopped	PSU							PSU temperature has probably increased
04	LOGIC	3.3V power voltage has dropped	LOGIC	PSU						
06		3.3V power startup is faulty	X-SUS	Y-SUS	ADM1-8	PSU	ABUS-L	ABUS-R	LOGIC	
08		1V power voltage has dropped	LOGIC	PSU						
0A		1V power startup is faulty	X-SUS	Y-SUS	ADM1-8	PSU	ABUS-L	ABUS-R	LOGIC	
18		Internal I2C_SCL1_LOW level	LOGIC							
19		Internal I2C_ACK does not respond	LOGIC							
1C		EEPROM initial setting is defective	LOGIC							
1D		EEPROM write-down is defective	LOGIC							
1E		EEPROM user initial setting is defective	LOGIC							
1F		EEPROM factory setting reading is defective	LOGIC							
24	X-SUS	Vex power voltage has decreased	X-SUS	LOGIC						
25		Vex power voltage is excessive	X-SUS							
26		Vex power startup is faulty.	X-SUS	LOGIC						
28		Vx power voltage has dropped	X-SUS	LOGIC						
29		Vx power voltage is excessive	X-SUS							
2A		Vx power startup is faulty.	X-SUS	LOGIC						
39		Vs power current is excessive (during operation)	X-SUS	Panel	LOGIC					
3B		Vs power current is excessive (during startup)	X-SUS	Panel	LOGIC					
44	Y-SUS	Vey power voltage has dropped	Y-SUS	LOGIC						
45		Vey power voltage is excessive	Y-SUS							
46		Vey power startup is faulty.	Y-SUS	LOGIC						
59		Vs power current is excessive (during operation)	Y-SUS	Panel	LOGIC					
5B		Vs power current is excessive (during startup)	Y-SUS	Panel	LOGIC					
5D		Vs power current is excessive (during operation)	Y-SUS	SDM	Panel	LOGIC				
61	X-SUS Y-SUS	Vs power voltage is excessive	PSU	LOGIC						
62		Vs power startup is faulty.	X-SUS	Y-SUS	PSU	LOGIC				
64		Vex and Vpy power voltage has dropped	LOGIC	X-SUS	Y-SUS					
65		Vex and Vey power voltage is excessive	X-SUS	Y-SUS						
66		Vex and Vey power startup is faulty.	LOGIC	X-SUS	Y-SUS					
68		Vw power voltage has dropped	Y-SUS	X-SUS	LOGIC					
69		Vw power voltage is excessive	X-SUS							
6A		Vw power startup is faulty.	Y-SUS	X-SUS	LOGIC					
81	ABUS	Va power voltage is excessive	PSU	LOGIC						
82		Va power startup is faulty.	ADM1-8	PSU	LOGIC	ABUS-L	ABUS-R			
99		Va power current is excessive (during operation)	ADM1-8	ABUS-L	ABUS-R	PSU	LOGIC			
9B		Va power current is excessive (during startup)	ADM1-8	ABUS-L	ABUS-R	PSU	LOGIC			

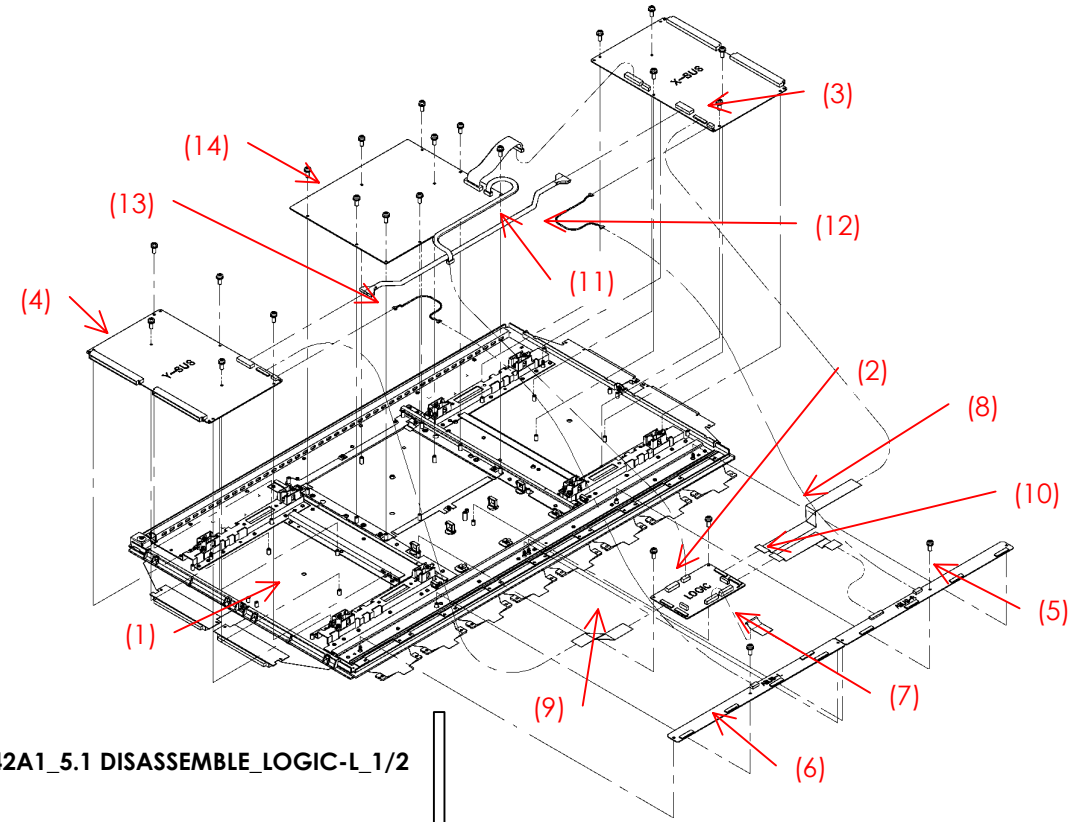
ERR code	Detect position (board)	Contents	Suspected faulty board (In the order of higher probability of defect)							Remarks
			(1)	(2)	(3)	(4)	(5)	(6)	(7)	
9D		Va power current is excessive (during operation)	ADM1-8	ABUS-L	ABUS-R	PSU	LOGIC			Excess current is detected in ACCC operation.
A5	ADM1	ADM1 has abnormal heat generation.	ADM1	PSU	LOGIC					It can possibly occur depending on screen display.
A9	ADM2	ADM2 has abnormal heat generation.	ADM2	PSU	LOGIC					
AD	ADM3	ADM3 has abnormal heat generation.	ADM3	PSU	LOGIC					
B1	ADM4	ADM4 has abnormal heat generation.	ADM4	PSU	LOGIC					
B5	ADM5	ADM5 has abnormal heat generation.	ADM5	PSU	LOGIC					
B9	ADM6	ADM6 has abnormal heat generation.	ADM6	PSU	LOGIC					
BD	ADM7	ADM7 has abnormal heat generation.	ADM7	PSU	LOGIC					
C5	ADM8	ADM8 has abnormal heat generation.	ADM8	PSU	LOGIC					
E2	LOGIC	5V power startup is faulty.	X-SUS	Y-SUS	PANEL	PSU	ABUS-L	ABUS-R	LOGIC	
FC	PSU	Detection error of Vs and Va voltage.	PSU	LOGIC						

5 DISASSEMBLING AND REASSEMBLING

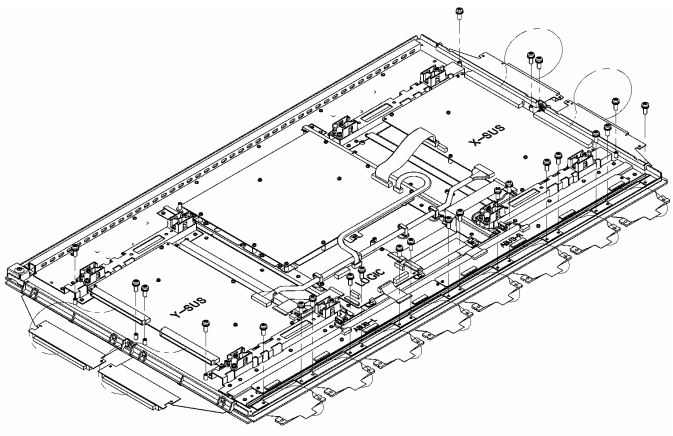
Unless otherwise specified, use the torque screwdriver for screw tightening, following the tightening torques below.

Screw size	Tightening torque
M 3	69±0.049Nm (7±0.5kg·cm)
M 4	1.18±0.098Nm (12±1.0kg·cm)

5.1 EXPLODED VIEW



42A1_5.1 DISASSEMBLE_LOGIC-L_1/2



42A1_5.1DISASSEMBLE_LOGIC-L_1/2

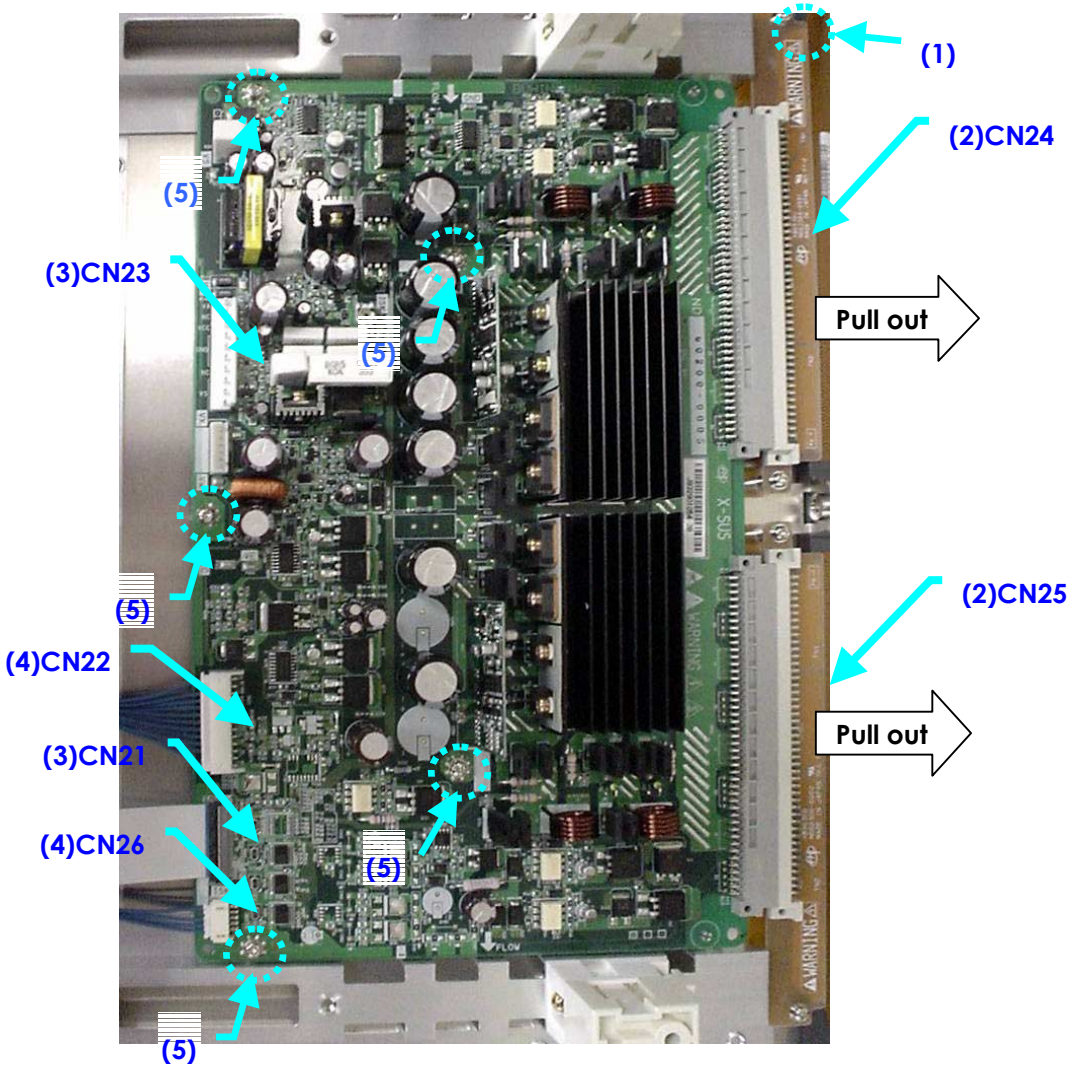
5.2 X-SUS CIRCUIT BOARD REMOVAL/INSTALLATION PROCEDURE

Note

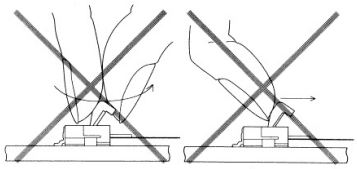
When removing the circuit board after the main power is turned on/off, wait for at least one minute before starting to remove the circuit board.
If the circuit board removal is started immediately after turning off the main power, it can result in electric shock or damage to the circuit due to residual electric charge.

Remove the circuit board following the steps below. To install the circuit board, reverse the removal procedure.

(1) Remove the fixing screws (M3x8) fixing XBB at 4 locations.
(2) Pull out the XBB board horizontally and disconnect the connectors (CN24, CN25).
(3) Release the lock of the FPC connector (CN21) and disconnect the signal cable.
(4) Disconnect the cables from the VH connectors (CN22, CN23).
(5) Remove the fixing screws (M3x8) fixing XSUS at 5 locations.



Note

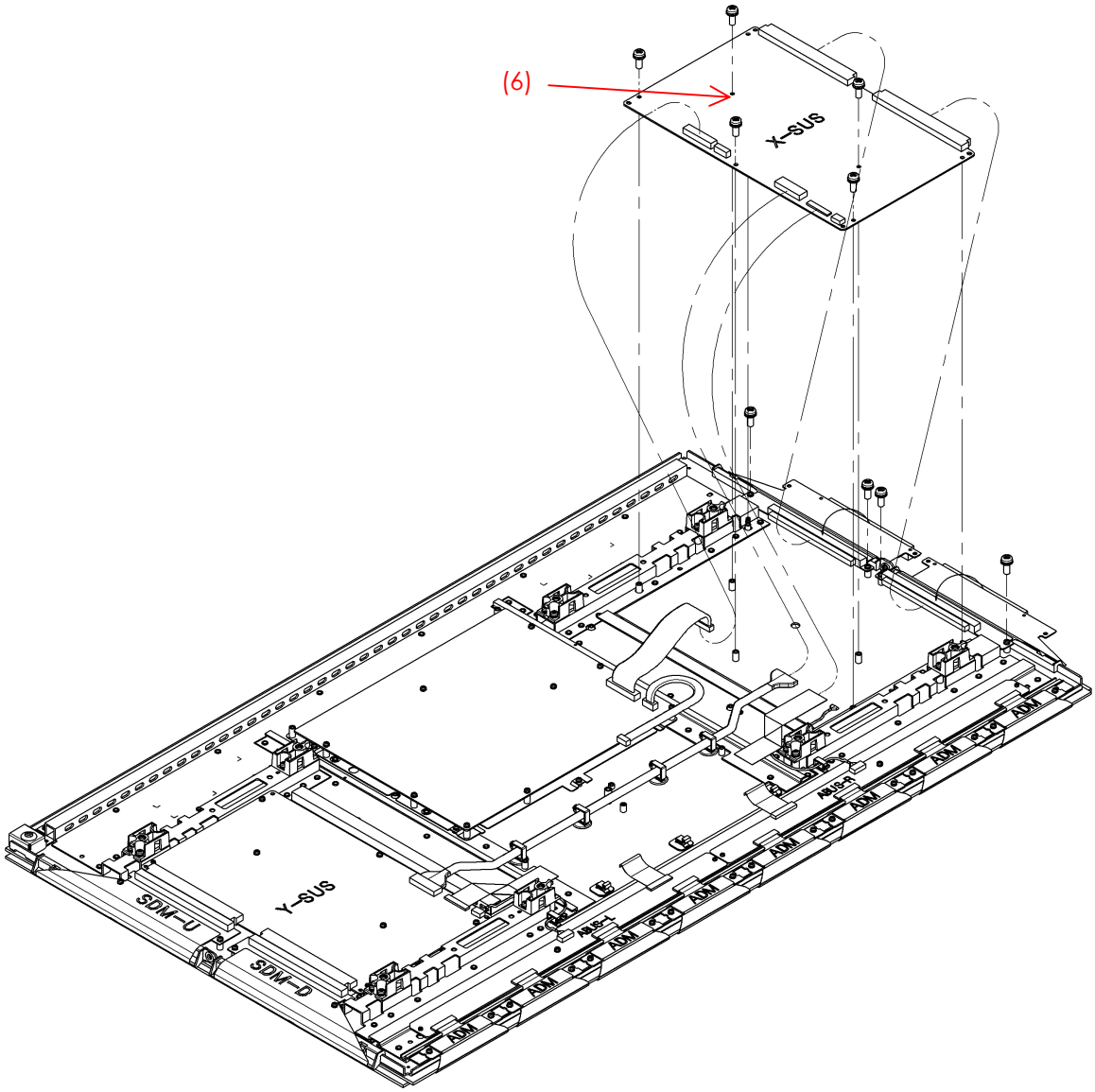


* On handling the FPC connector

To release the lock, release it by gently flipping it with the nail of the thumb or forefinger.

Never pinch the lock lever with fingers or hook on it (especially with a fingernail). Doing so might damage the lock lever.

(6) Remove the X-SUS board.
Make sure that you do not to hold the heat sink when removing the Y-SUS board.



42A1_5. 2 (5) X-SUS

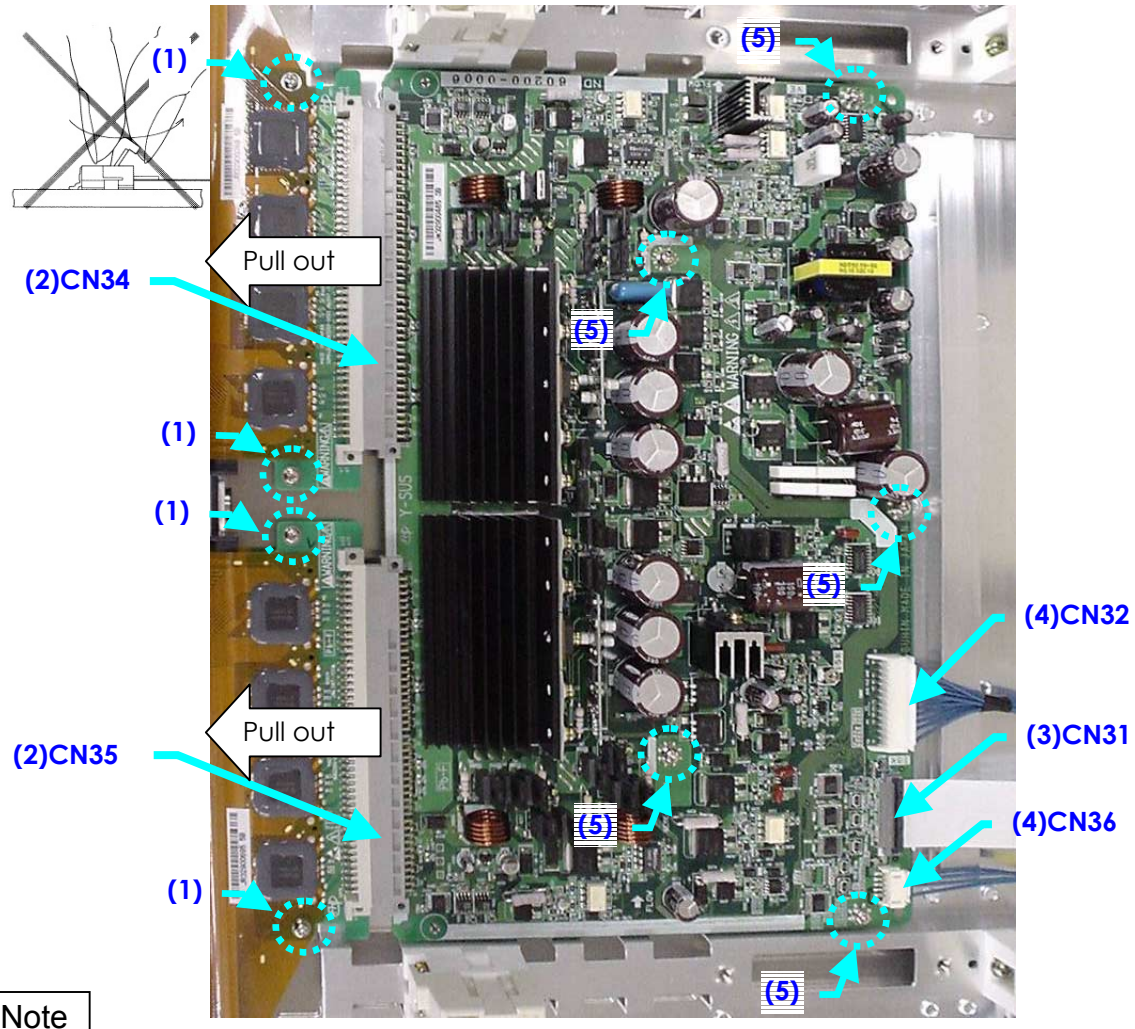
5.3 Y-SUS CIRCUIT BOARD REMOVAL/INSTALLATION PROCEDURE

Note

When removing the circuit board after the main power is turned on/off, wait for at least one minute before starting to remove the circuit board.
If the circuit board removal is started immediately after turning off the main power, it can result in electric shock or damage to the circuit due to residual electric charge.

Remove the circuit board by following the steps below. To install the circuit board, reverse the removal procedure.

(1) Remove the fixing screws (M3x8) fixing SDM at 4 locations.
(2) Pull out the SDM board horizontally and disconnect the connectors (CN34, CN35).
(3) Release the lock of the FPC connector (CN31) and disconnect the signal cable.
(4) Disconnect the cables from the VH connectors (CN32, CN33).
(5) Remove the fixing screws (M3x8) fixing YSUS at 5 locations.



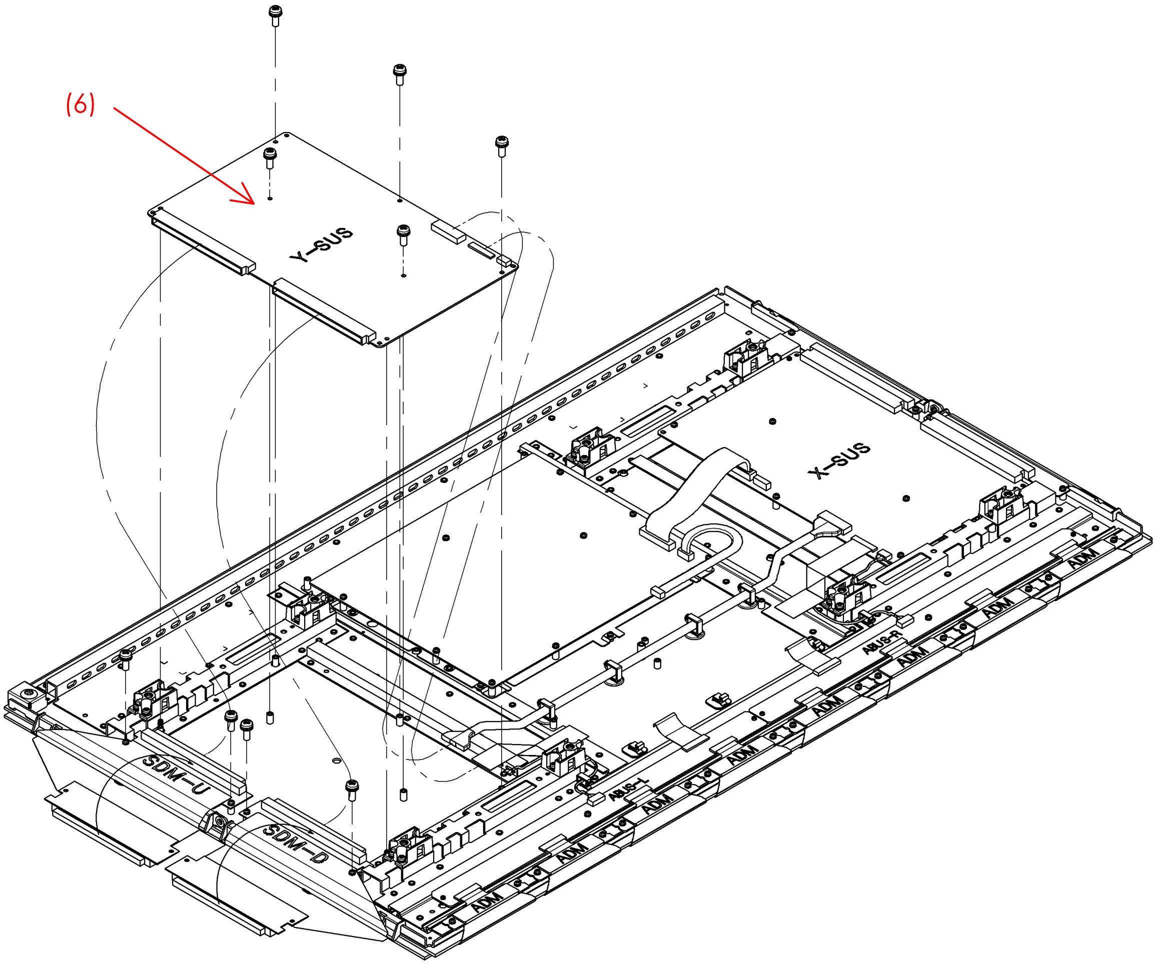
Note

* On handling the FPC connector

To release the lock, release it by gently flipping it with the nail of the thumb or forefinger.
Never pinch the lock lever with fingers or hook onto it (especially with fingernails). Doing so might damage the lock lever.

(6)Remove the Y-SUS board.

Make sure that you do not to hold the heat sink when removing the Y-SUS board.



42A1_5. 3 (6) Y-SUS

5.4 ABUS-L CIRCUIT BOARD REMOVAL/INSTALLATION PROCEDURE

Note

When removing the circuit board after the main power is turned on/off, wait for at least one minute before starting to remove the circuit board.
If the circuit board removal is started immediately after turning off the main power, it can result in electric shock or damage of the circuit due to residual electric charge.

Remove the circuit board by following the steps below. To install the circuit board, reverse the removal procedure.

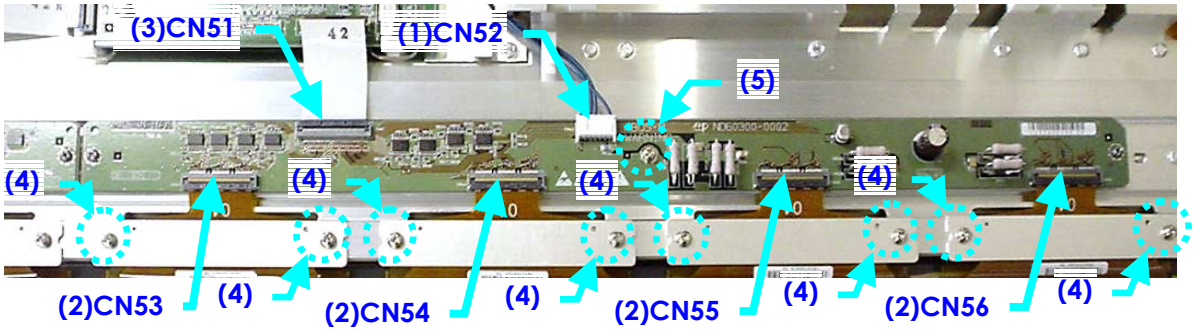
(1) Disconnect the connector CN52 from the ABUS-L board.

(2) Raise the lock of the FPC connectors CN53, CN54, CN55 and CN56 to release it and remove the ADM flexible board.

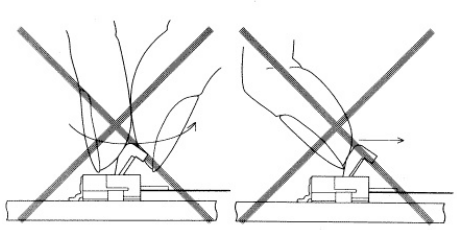
(3) Release the lock of the FPC connector CN51 and disconnect the signal cable (FPC).

(4) Remove the screws (M3x8) fixing the ADM at the 8 locations.

(5) Remove the screws (M3x8) fixing the ABUS-L board at the 1 location.



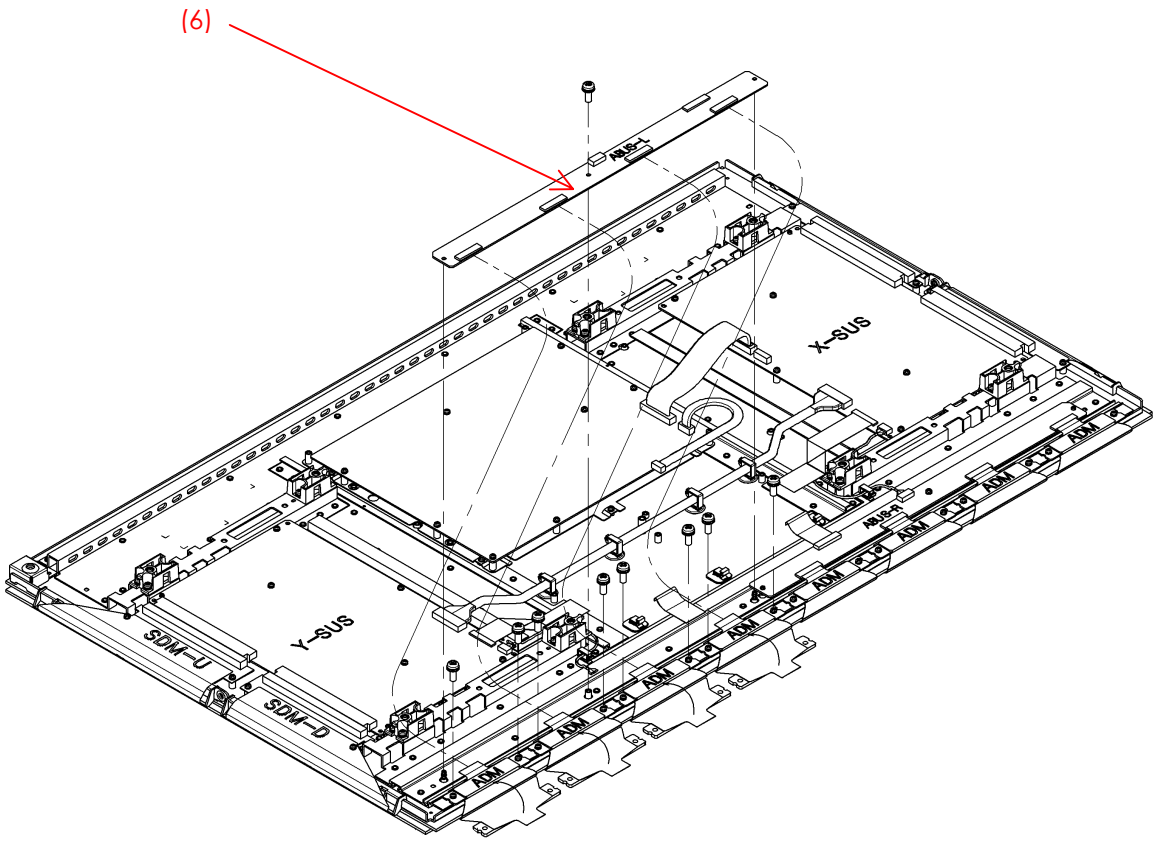
Note



* On handling the FPC connector
To release the lock, release it by pulling up the lever.
Never pinch the lock lever with the fingers or push hard on it without a cable in it. Doing so might damage the lock lever.

(6) Remove the ABUS-L board

(7) When installing the ABUS-L board, place it so that the ABUS-L board is locked by the tabs for fixing it in position.



42A1_5. 4 (4)~(7) ADM, AbusL

5.5 ABUS-R CIRCUIT BOARD REMOVAL/INSTALLATION PROCEDURE

Note

When removing the circuit board after the main power is turned on/off, wait for at least one minute before starting to remove the circuit board.
If the circuit board removal is started immediately after turning off the main power, it can result in electric shock or damage of the circuit due to residual electric charge.

Remove the circuit board by following the steps below. To install the circuit board, reverse the removal procedure.

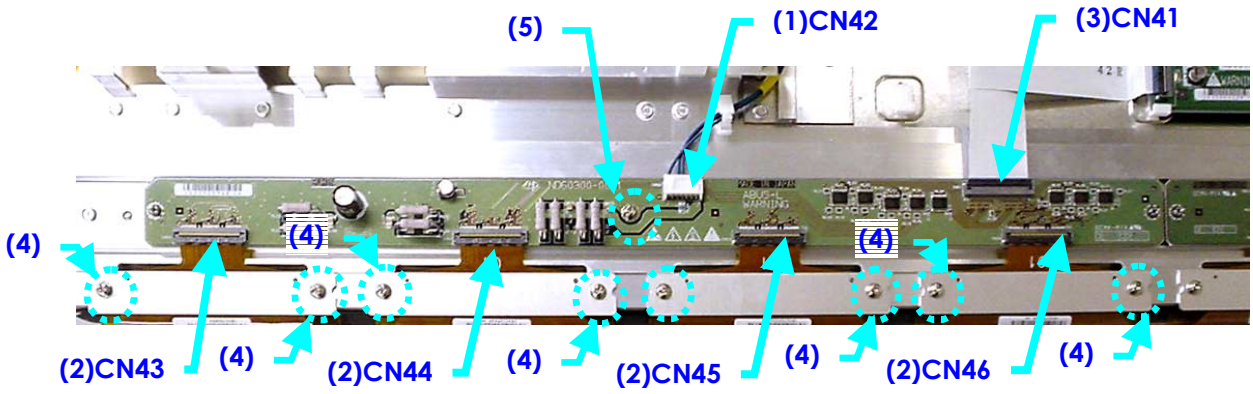
(1) Disconnect the connector CN42 on the ABUS-R board.

(2) Raise the lock of the FPC connectors CN43, CN44, CN45, CN46 to release it and disconnect the ADM flexible board.

(3) Release the lock of the FPC connector CN41 and disconnect the signal cable (FPC).

(4) Remove the screws (M3X8) fixing the ADM at the 8 locations.

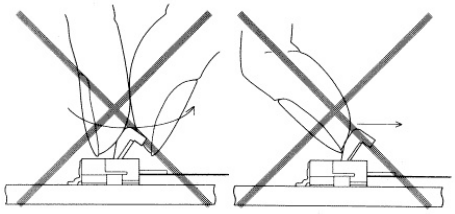
(5) Remove the screws (M3X8) fixing the ABUS-R board at the 1 locations.



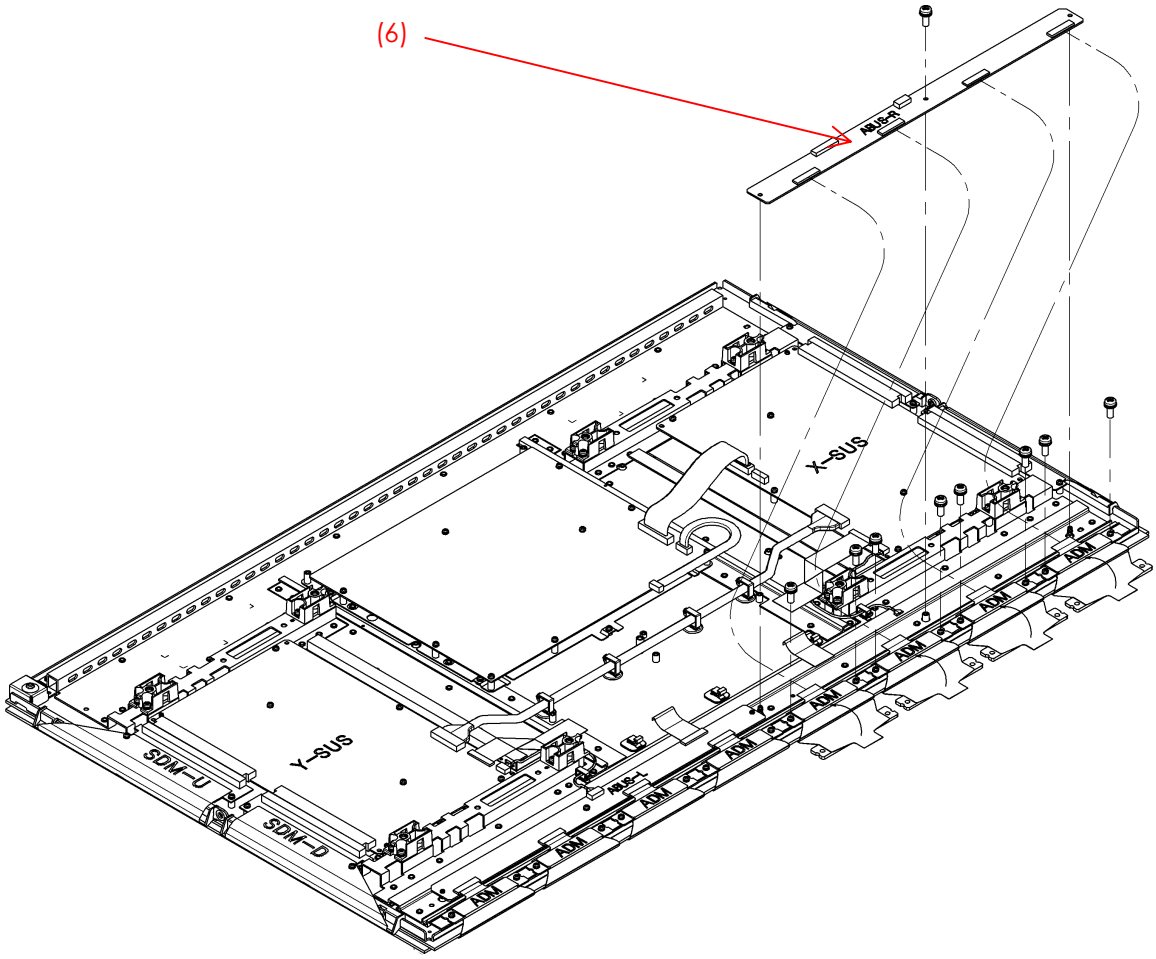
Note

* On handling the FPC connector

To release the lock, release it by pulling up the lever. Never pinch the lock lever with the fingers or push hard on it without a cable in it. Doing so might damage the lock lever.



(6) Remove the ABUS-R board.
When installing the ABUS-R board, place it so that the ABUS-R board is locked by the tabs for fixing it in position.



42A1_5. 5 (4)~(7) ADM, AbusR

5.6 LOGIC BOARD REMOVAL/INSTALLATION PROCEDURE

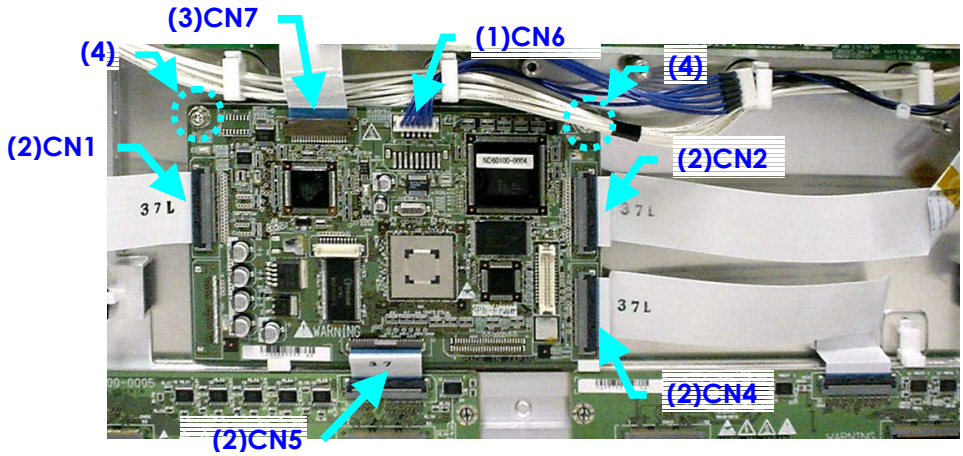
Remove the circuit board by following the steps below. To install the circuit board, reverse the removal procedure.

(1) Disconnect the EH connector CN6.

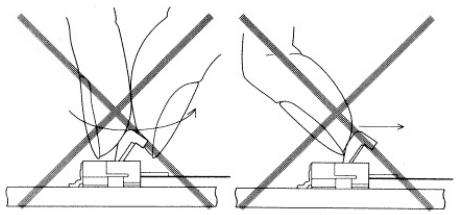
(2) Release the lock of the FPC connectors CN1, CN2, CN4, CN5 and disconnect the signal cable (FPC).

(3) Slide the lock of the FPC connector CN7 toward the PSU board side, then press it down toward the front and remove the PSU signal cable.

(4) Remove the screws (M3x8) fixing the LOGIC board in position at 2 locations.



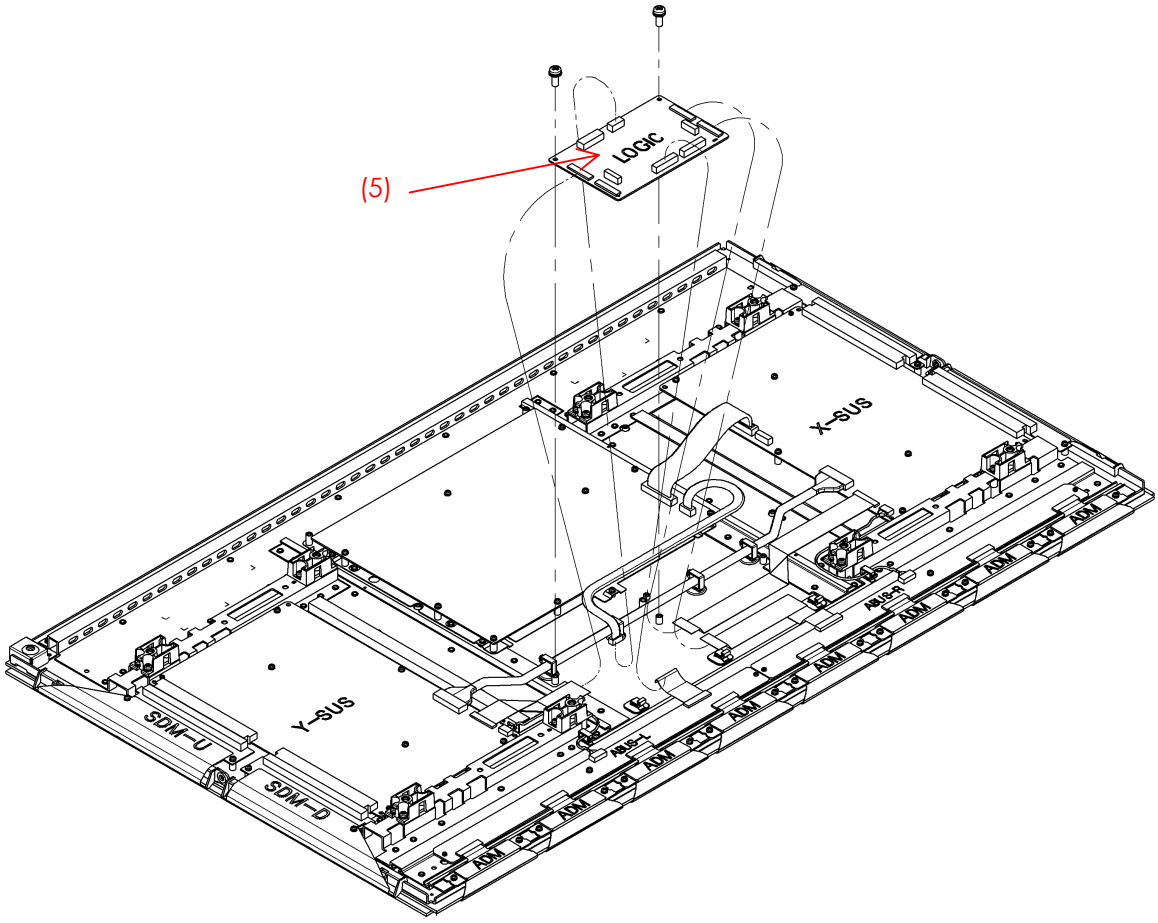
Note



* On handling the FPC connector
To release the lock, release it by gently flipping it.
Never pinch the lock lever with the fingers or hook onto it (especially with fingernails). Doing so might damage the lock lever.

(5) Remove the LOGIC board.

(6) When installing the LOGIC board, place it so that the LOGIC board is locked by the tabs for fixing it in position (at 2 locations).



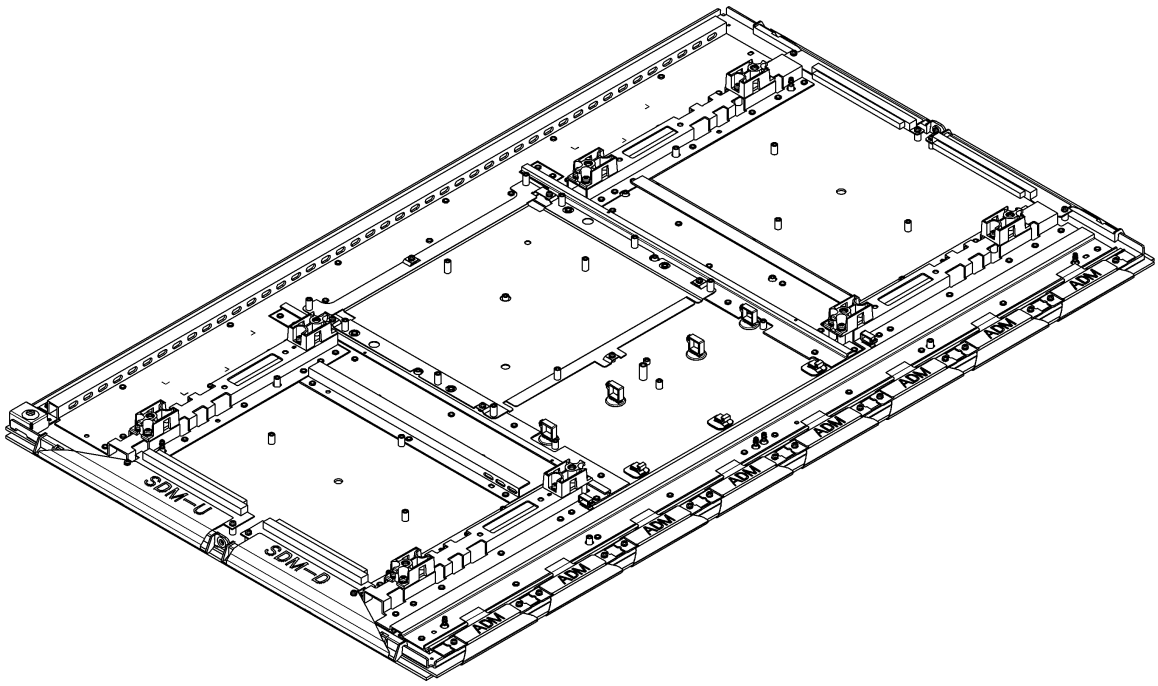
42A1_5. 6 (4)~(6) LOGIC-L

5.7 COMPLETE PANEL CHASSIS REMOVAL/INSTALLATION PROCEDURE

(1) Remove the 6 types of printed-circuit board (X-SUS, Y-SUS, ABUSL, ABUSR, LOGIC, PSU) that are installed in the panel module.

For the removal procedure, refer to Section 5.2 to 5.7.

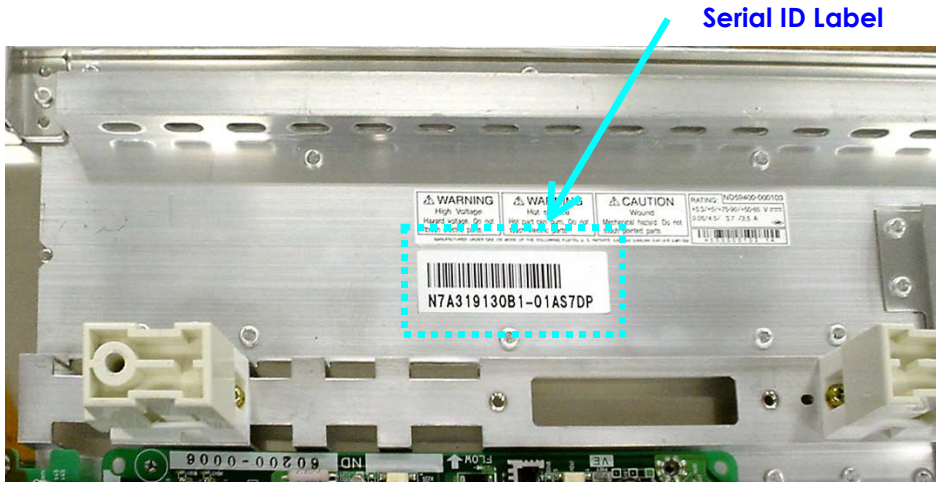
* Before removing the above 6 types of board, be sure to remove both ends of the single power cable (BLU) and those of the five FPC cables (WHT) that are used to connect the circuit boards.

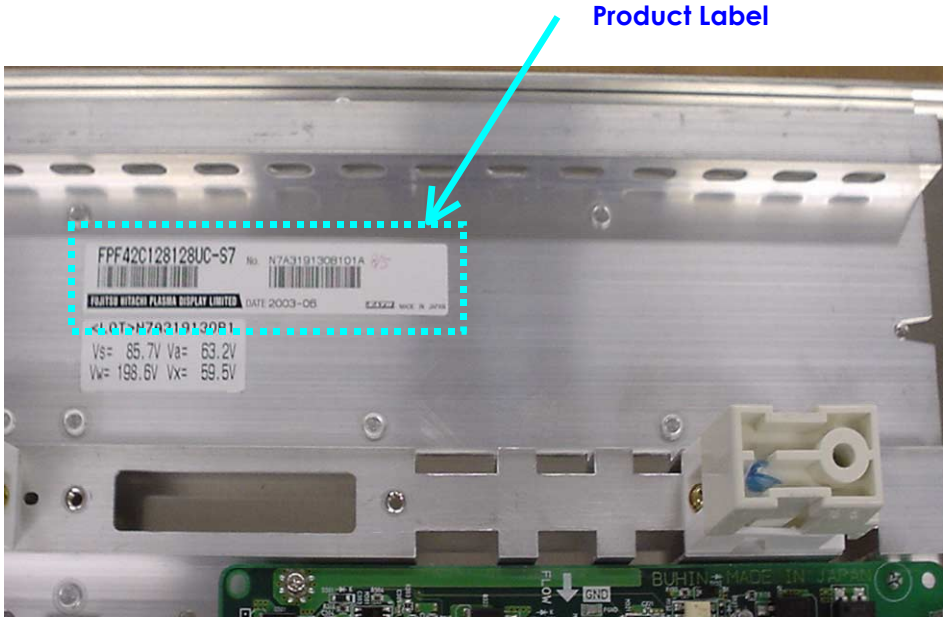


42A1_5. 8 COMPLETE PANEL CHASSIS REMOVAL

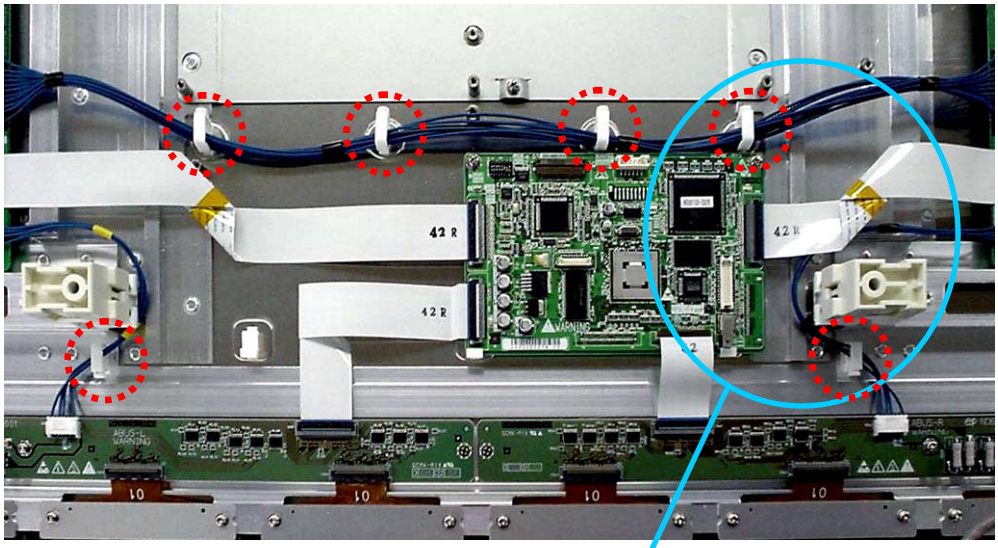
(2) ***Install the printed-circuit board that was removed in step (1) and fix it in position. (Refer to the exploded view shown in Section 5.1.)

(3) Print the serial ID number of the product to be repaired on the product label which is prepared separately. Attach the product label to the panel chassis on top of the Y-SUS board (See the photo).

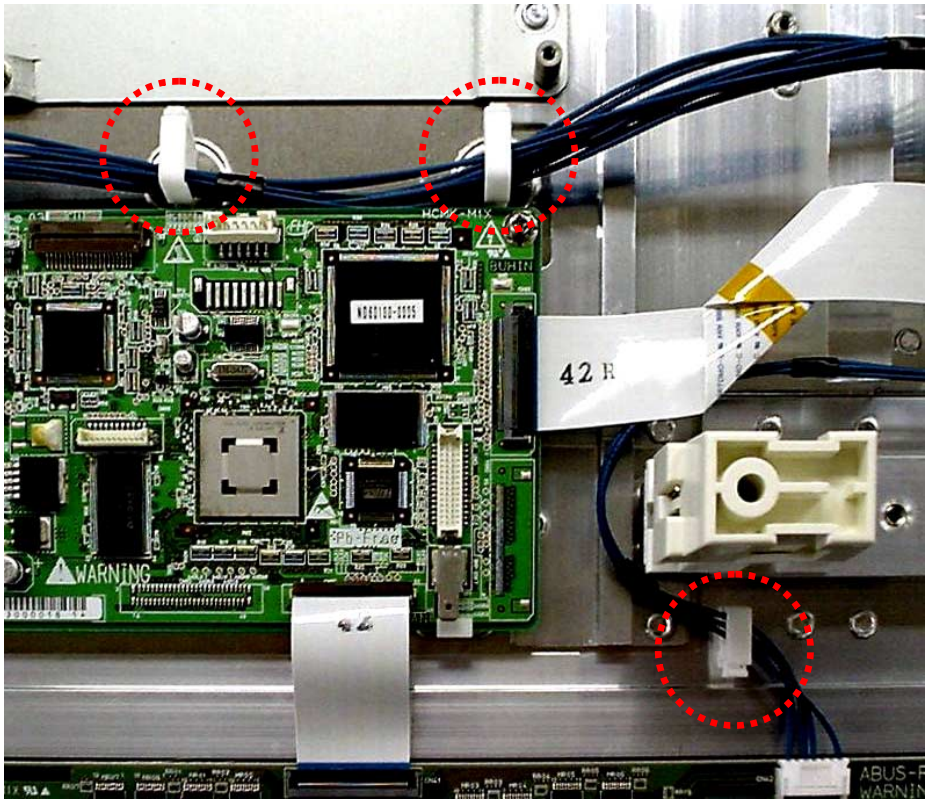




(4) When the installation of the board is complete, route the wires as shown below.



Enlarge



6 OPERATION CHECK AND ADJUSTMENT METHOD

6.1 LIST OF CHECK AND ADJUSTMENT ITEMS

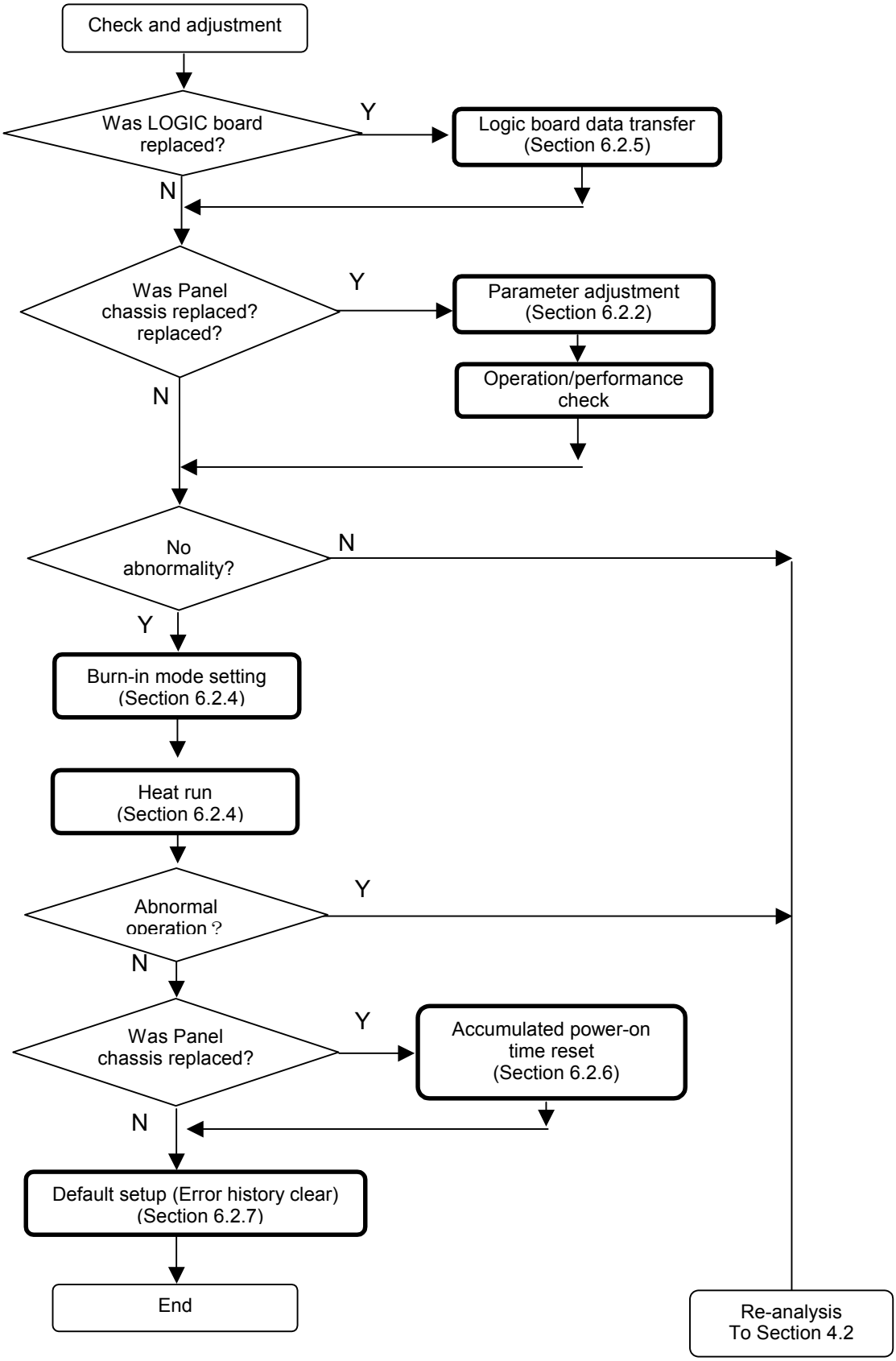
Adjustment item (Major item)	Adjustment item (Minor item)	Adjustment position (Name of the part)	Check and adjustment Required timing						Jig/tools	Labor required	
			When PDP panel is replaced	When X-SUS board is replaced	When Y-SUS board is replaced	When LOGIC board is replaced	When ABUS board is replaced	When PSU board is replaced		Labor (persons)	Time (minutes)
VR adjustment	Is detection adjustment	X-SUS board VR1							Digital voltmeter , screwdriver	1	1
	Ve voltage adjustment	X-SUS board VR4								1	1
	Vw voltage adjustment	X-SUS board VR3								1	1
	Ve voltage adjustment	Y-SUS board VR1								1	1
	Is detection adjustment	Y-SUS board VR2								1	1
	PFC voltage adjustment	PSU board RV301								1	1
	Vs adj1	PSU board RV801								1	1
	Vs adj2	PSU board RV802								1	1
	Va adj2	PSU board RV803								1	1
	Vs f min	PSU board RV901								1	1
	Vpr adj	PSU sub-board RV201								1	1
	Vcc f min	PSU sub-board RV150								1	1
	Vcc adj	PSU sub-board RV270								1	1
	Va adj1	PSU sub-board RV860								1	1
	Vaa	PSU sub-board RV861								1	1
	Va f min	PSU sub-board RV950								1	1
Parameter adjustment	Vs voltage adjustment	LOGIC board(Vsvolt)	○			○			Interface board, personal computer, Digital voltmeter	1	1
	Va voltage adjustment	LOGIC board(Vavolt)	○			○				1	1
	Vw voltage adjustment	LOGIC board(Vwvolt)	○			○				1	1
	Vx voltage adjustment	LOGIC board(Vxvolt)	○			○				1	1
Default setting	Error history clear	LOGIC board (EEPROM)	○	○	○	○	○	○	Interface board, personal computer	1	1
	Accumulated power-on time clear	LOGIC board (EEPROM)	○							1	1

Be sure to keep the default setup set at the factory.
(Do not change the VR control settings.)

○ : Check, adjustment, or setup

6.2 CHECK AND ADJUSTMENT METHOD

6.2.1 Check and adjustment procedure

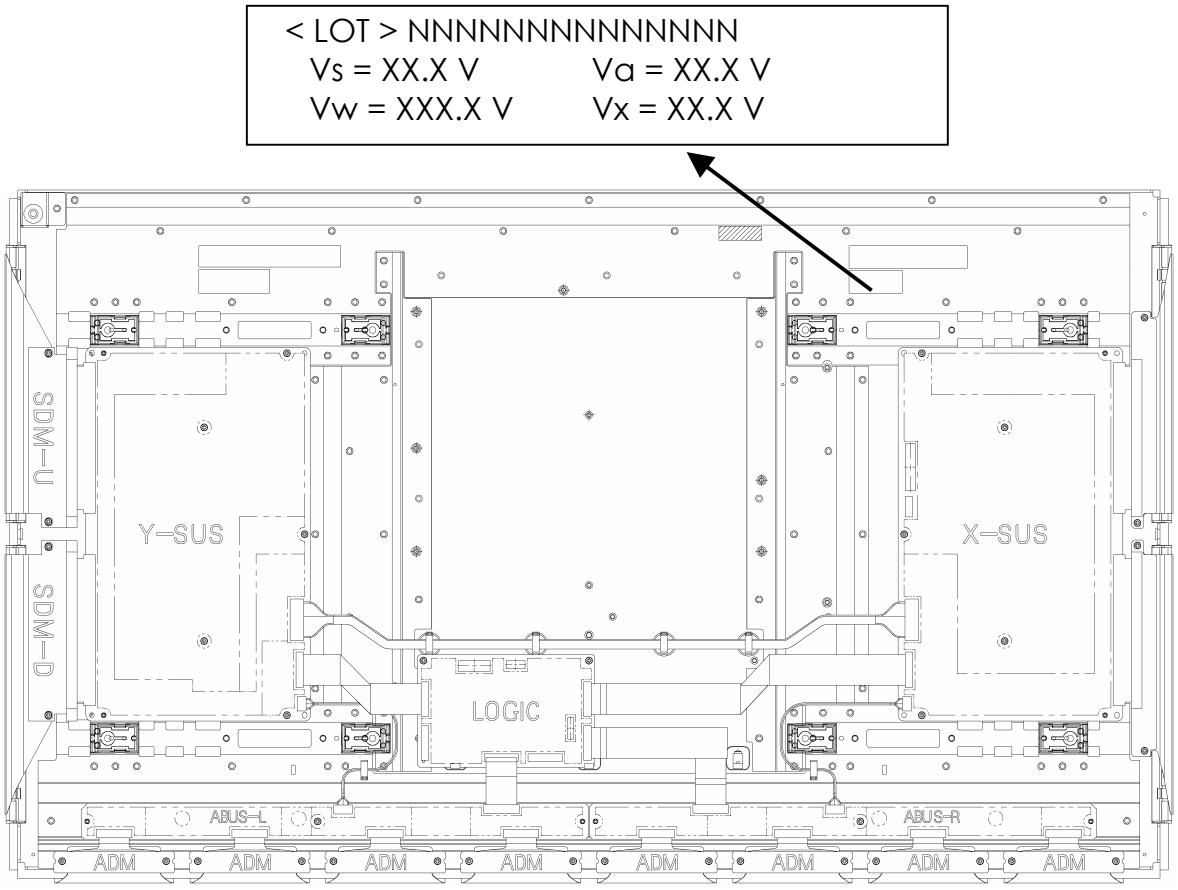


6.2.2 Parameter adjustment

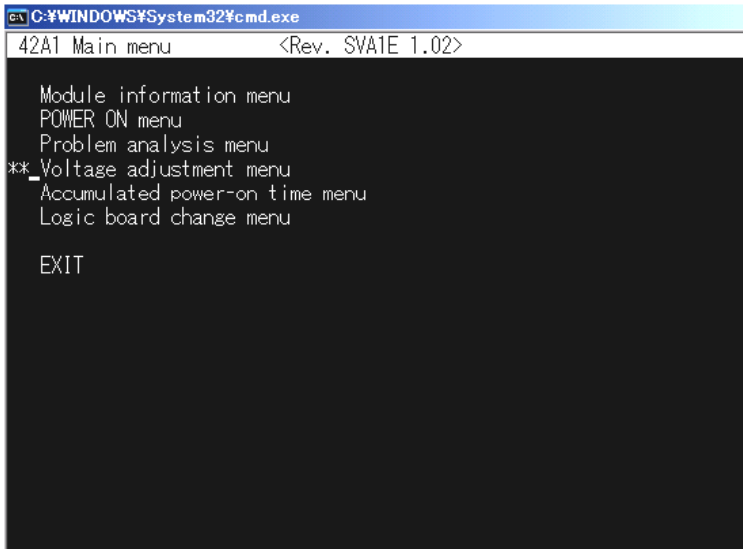
List of parameter adjustment items

Item	Adjustment items	Measurement point	Adjustment value (conditions)	Remarks
1	Vs voltage adjustment	X-SUS board PVS	Voltage setting label indication value* ; ±1% (all black)	
2	Va voltage adjustment	X-SUS board PVA	Voltage setting label indication value* ; ±1% (all black)	
3	Vw voltage adjustment	X-SUS board PVW	Voltage setting label indication value* ; ±1% (all black)	
4	Vx voltage adjustment	X-SUS board PVX	Voltage setting label indication value* ; ±1% (all black)	

*: Voltage setting label shows the following messages at the top left of the back of the chassis.

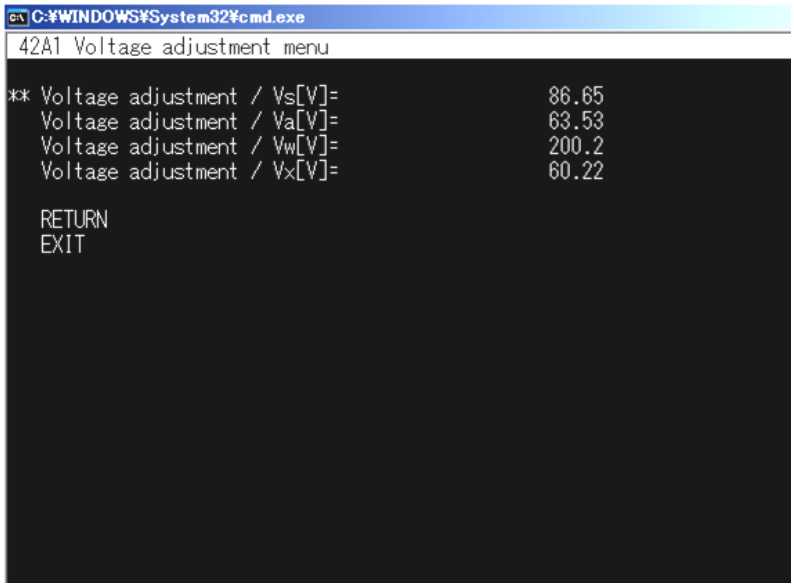


(1) From the main menu, select the voltage adjustment menu with the ↑ key or ↓ key and press the <ENTER> key.



(2) From the voltage adjustment menu, adjust parameters in the order starting from Vs, Va, Vw, and Vx.

Select parameter with the ↑ key or ↓ key and adjust the parameter with the → key (increment) or ← key (decrement). The adjustment values are shown on the voltage label that is attached to the panel chassis.



** numbers are shown in decimal values.

Input the numeric value/dot and press the <ENTER> key and then press the <ENTER> key again to set the adjustment value directly.

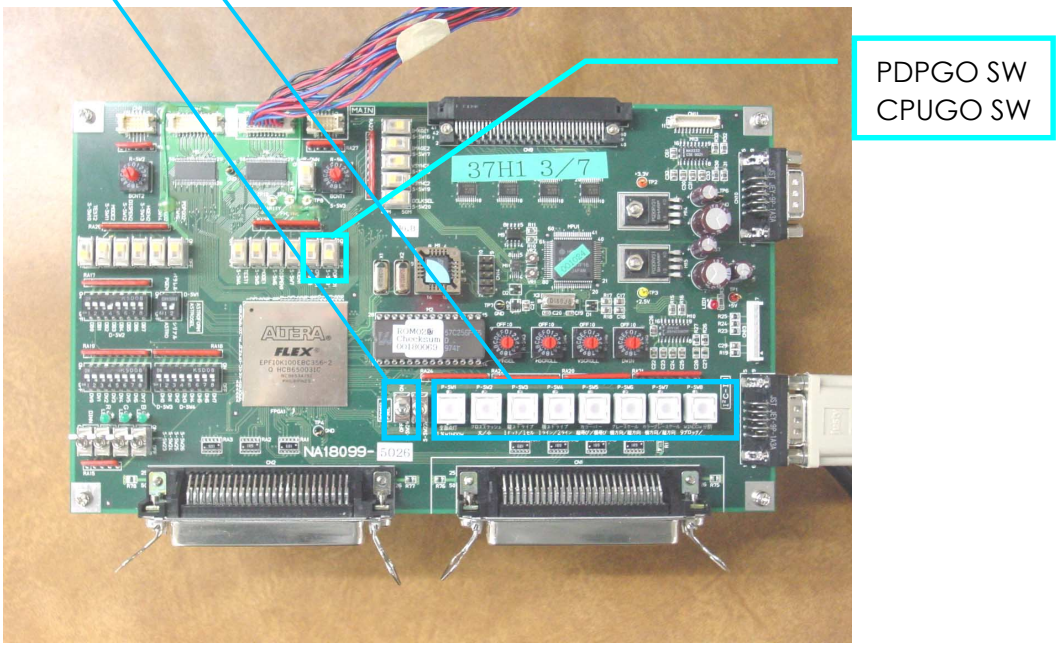
(3) Select RETURN with the ↑ key or ↓ key and press the <ENTER> key to return to the menu screen.

6.2.3 Operation performance check items

(1) Environmental conditions
Temperature: Room temperature
Judgment distance: 1 meter from panel screen
Preheat run: 5 minutes with entire screen lit (white)

(2) Test patterns:

PSEL	Push SW	Display pattern	Size	Details
H	0	White screen		
H	1	Cross slash	Large	24 × 24
H	2	Vertical stripe	Every other dot	
H	3	Horizontal stripe	Every other line	
H	4	Color bars	Vertical bar	H_blk divided in 8
H	5	Gray scale	Horiz. direction	Every 3 dots
H	6	Color gray scale	Horiz. direction	Every 3 dots
H	7	Divided WINDOW	9 blocks	Follow the ROM
L	0	1% WINDOW	Center	Follow the ROM
L	1	Cross slash	Small	12 × 12
L	2	Vertical stripe	Every other cell	
L	3	Horizontal stripe	Every 2 lines	
L	4	Color bars	Horizontal bar	V_blk divided in 8
L	5	Gray scale	Vert. direction	Every 4 dots
L	6	Color gray scale	Vert. direction	Every 4 dots *2
L	7	Divided WINDOW	16 blocks	Follow ROM *3



(3) Judgment

Item	Test items	Test signal	Judgment criterion
1	Brightness non-uniformity	White screen (W)	Brightness non-uniformity in the form of stripes must not be visible in vertical and horizontal directions.
2	Black noise	Horizontal gray scale (Each color of R/G/B)	Rank 3 or higher in the 5-step evaluation. <Rank> 5: No noise 4: Small noise is intermittently visible 3: Noise of 1 line is not visible continuously 2: Noise occurs continuously 1: Much noise occurs continuously
3	Number of defects	The entire screen lights (Each color of W/R/G/B)	Conforms to Section 1.3.2 Display quality specifications. However, when Delivery Specifications Sheets are prepared for each client, the specifications shown in the Delivery Specifications Sheet must be met.
4	Number of extra dots		
5	Number of flickering dots		

(4) Power ON/OFF

*Power ON

Set both PDPGO-SW and CPUGO-SW to CN.

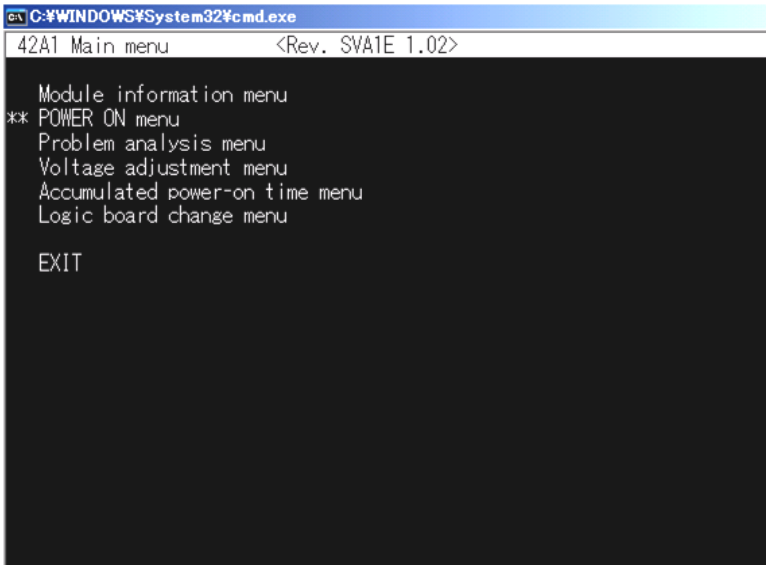
*Power OFF

Set only PDPGO-SW to OFF.(The CPUGO-SW remains ON.)

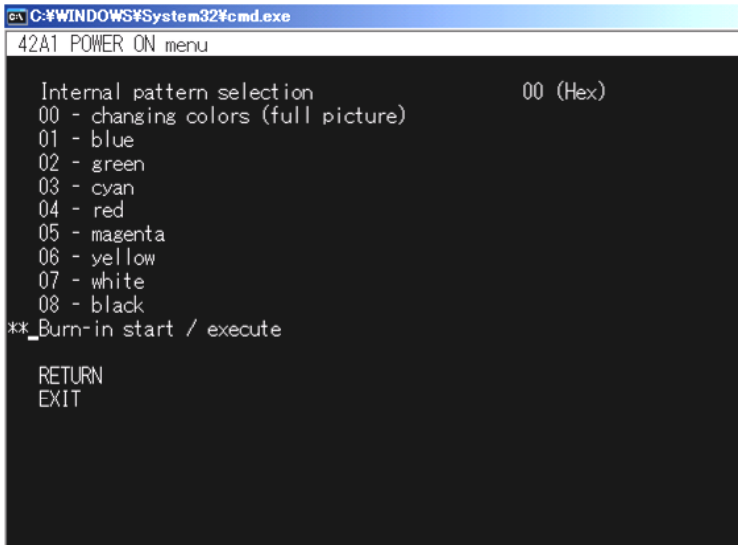
6.2.4 Heat Run Test

(1) Set the module by following the same procedure as that for Problem Analysis in Section 4.7.

(2) From the main menu, select the POWER ON menu with the ↑ key or ↓ key and press the <ENTER> key.



(3) From the POWER ON menu, select Internal pattern generation with the ↑ key or ↓ key and press the <ENTER> key. When you press the → key, the main power of the module is turned on. (When you press the ← key, the main power is turned off.)



(4) To change the internal pattern, select the internal pattern selection from the POWER ON menu using the ↑(up) or ↓(down) key, and press the <ENTER> key.

Setup value	Display pattern	Setup value	Display pattern
00	01 to 08 patterns are displayed every 2 seconds.	05	Entire screen is cyan
01	Entire screen is blue	06	Entire screen is yellow
02	Entire screen is red	07	Entire screen is white
03	Entire screen is magenta	08	Entire screen is black
04	Entire screen is green	F6	Plant burn-in pattern

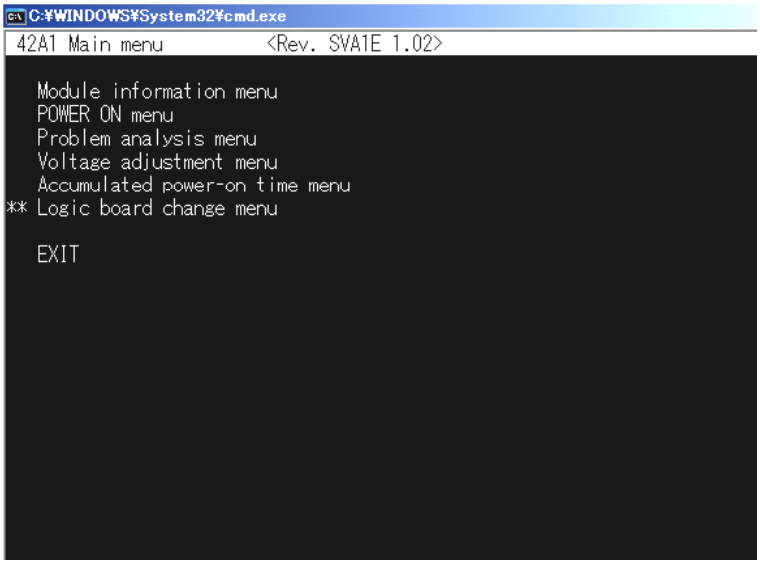
From the POWER ON menu, select Burn-in start with the ↑ key or ↓ key and press the <ENTER> key. The display pattern is automatically generated in PDP.

(6) Select RETURN with ↑ key or ↓ key and press <ENTER> key to return to the menu screen.

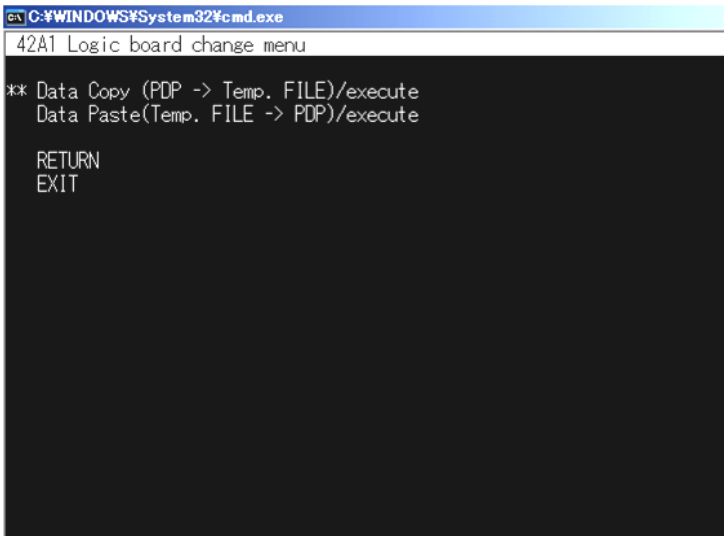
6.2.5 Logic board parameter forwarding

(1) The module is set according to the same to failure analysis procedure in clause 4.7. The logic board before being exchanged is installed in the module.

(2) From the main menu, select change Logic board menu with the ↑ key or ↓ key and press the <ENTER> key.

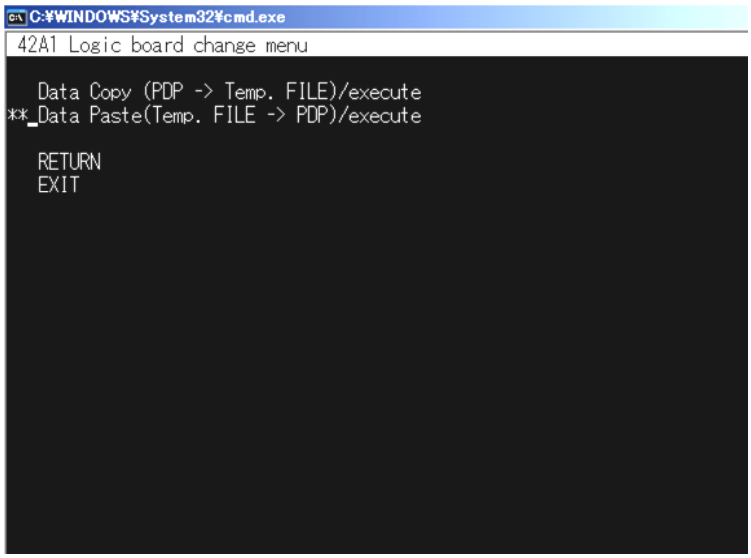


(3) From the logic board change menu, select data copy with the ↑ key or ↓ key and press the <ENTER> key. Data is read before the Logic board is exchanged.



(4) The Logic board is exchanged.

(5) From the logic board change menu, select data paste with the ↑ key or ↓ key and press the <ENTER> key. Data is written in the exchanged Logic board.

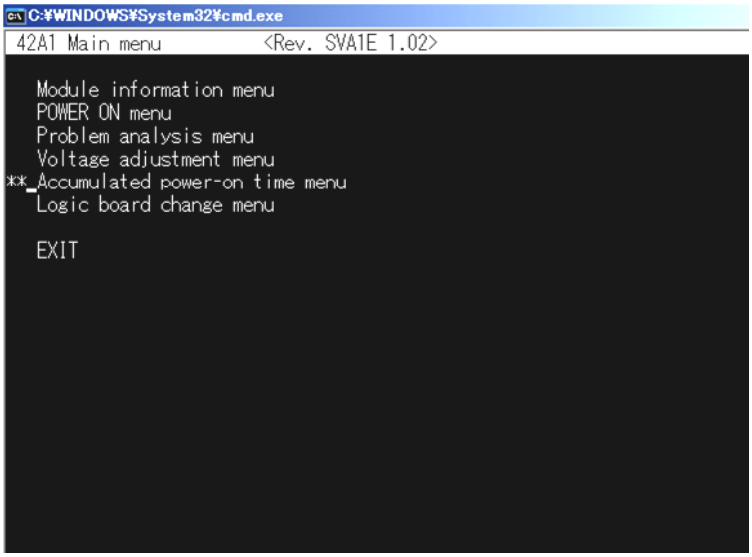


(6) Select RETURN with ↑ key or ↓ key and press <ENTER> key to return to the menu screen.

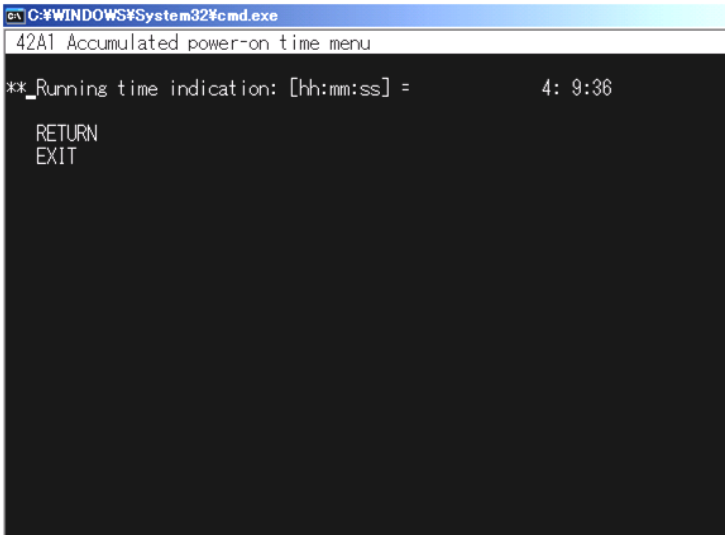
6.2.6 Accumulation time reset

(1) The module is set according to the same to failure analysis procedure in clause 4.7.

(2) From the main menu, select Power-on time menu with the ↑ key or ↓ key and press the <ENTER> key.



(3) From the Power-on time menu, select Operation hours with the ↑ key or ↓ key and press the <ENTER> key. The Operation hour is input. *It is not possible to change in the energizing time according to the version of the service software.



(4) "minute" is continuously input and < ENTER > key is pushed.

(5) "Second" is continuously input and < ENTER > key is pushed.

(6) Select RETURN with ↑key or ↓key and press <ENTER> key to return to the menu screen.

6.2.7 Setup before shipment

Before shipment from service, perform the following setup or initialization.

1) Initial values that are shown in the List of EEPROM contents in Section 3.3.1.
(Main power of the module is turned off.)
Clearing the error codes

From the each menu, select EXIT menu with the ↑ key or ↓key and press the <ENTER> key.

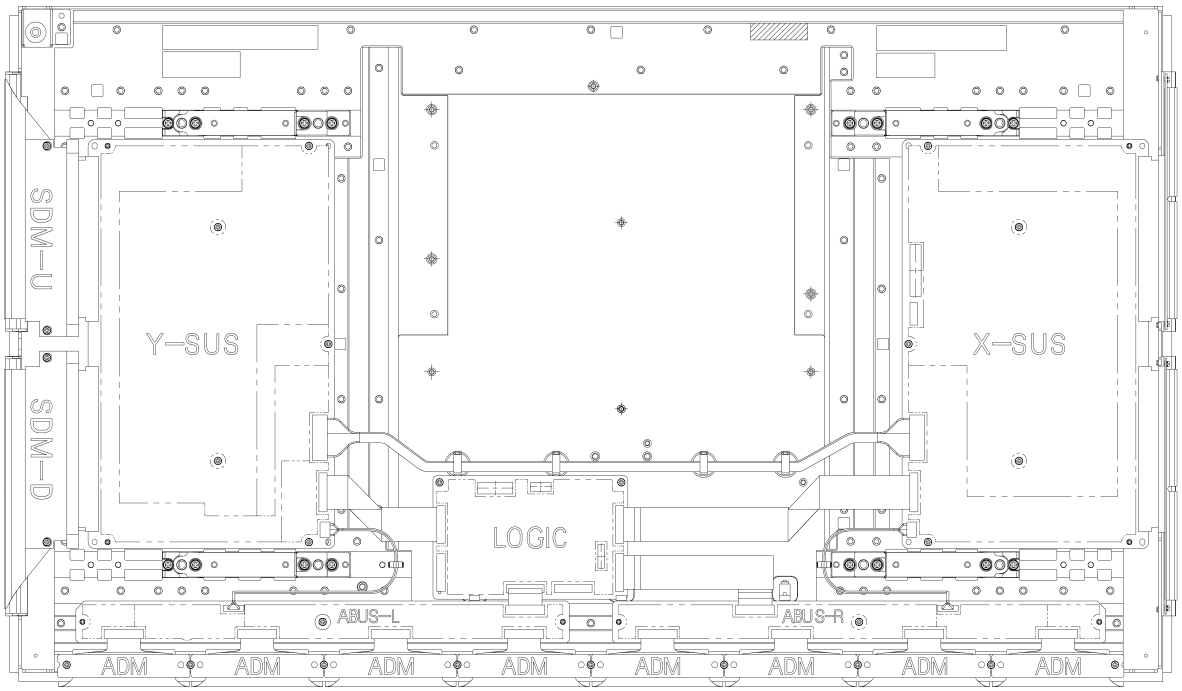
Shipping the set screen is displayed, and “Y" is pushed.
In shipping the set processing, there is a thing that the power supply of the module turns on automatically.
The shipment setting ends, and when the power supply of the module is on, the power supply is turned off automatically.

Shipment from service setting?(input the "Y" or "N" key)

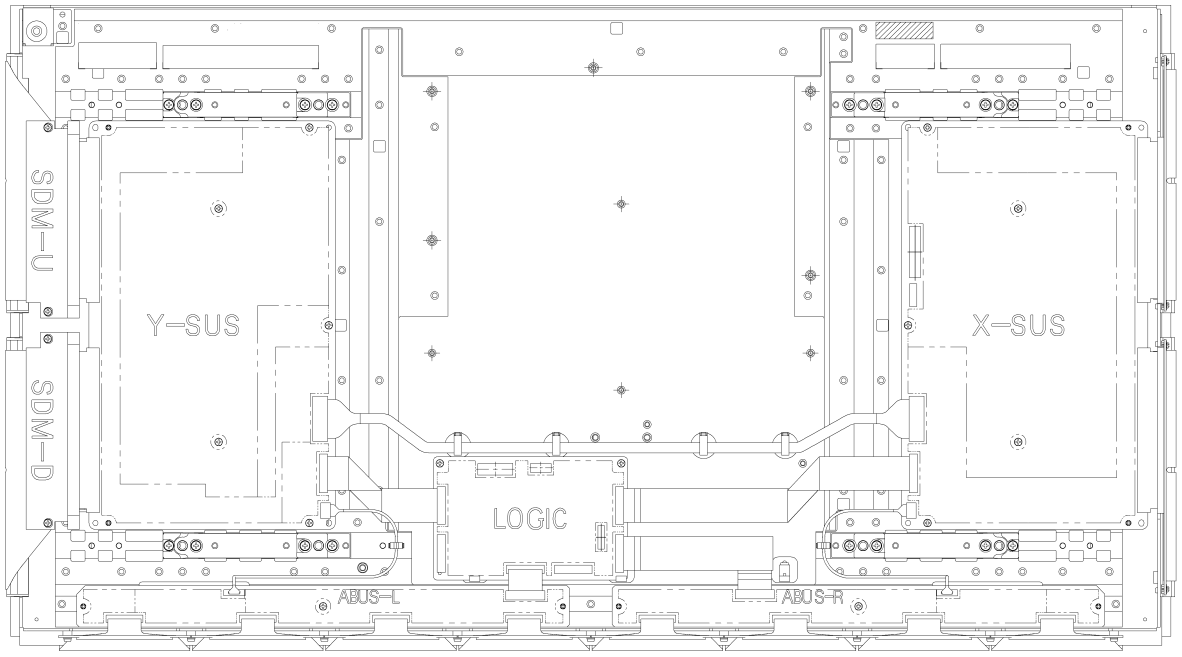
“N" When the key is pushed, the shipment setting is not done, and the power supply is turned off.

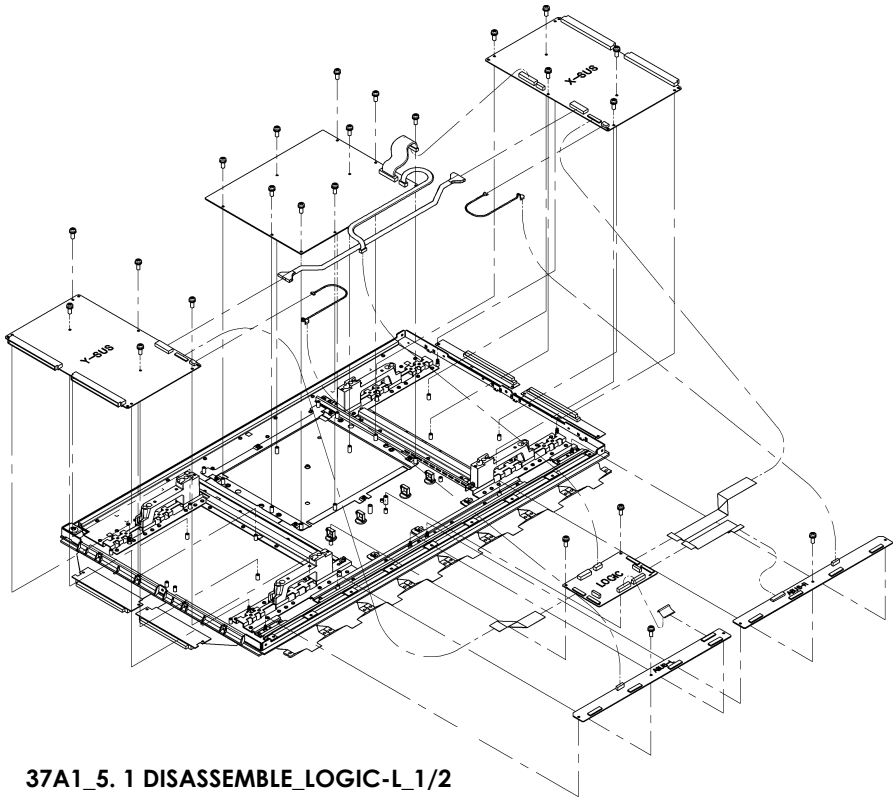
7 37A1 Mechanical Drawing

(1) FPF37C128128UB- 63

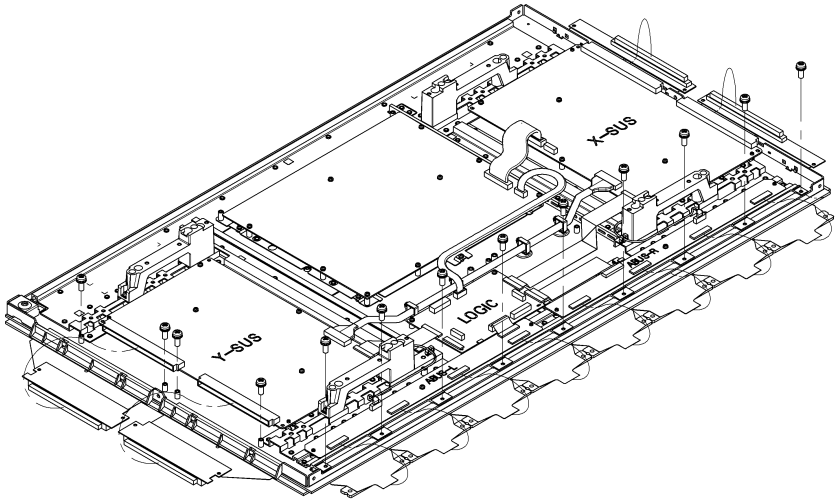


(2)FPF37C128128UB- 73

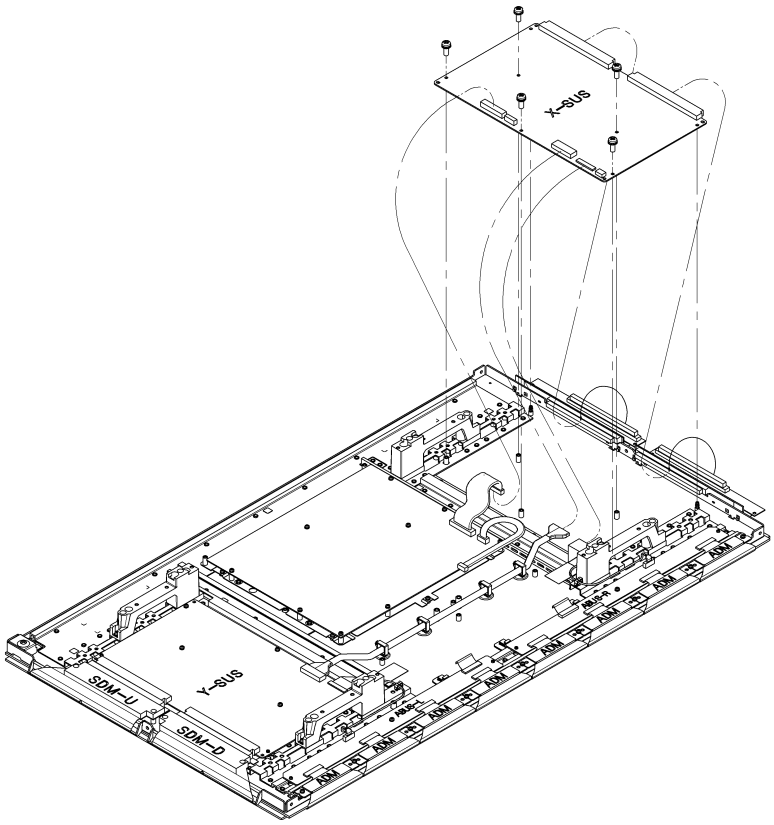




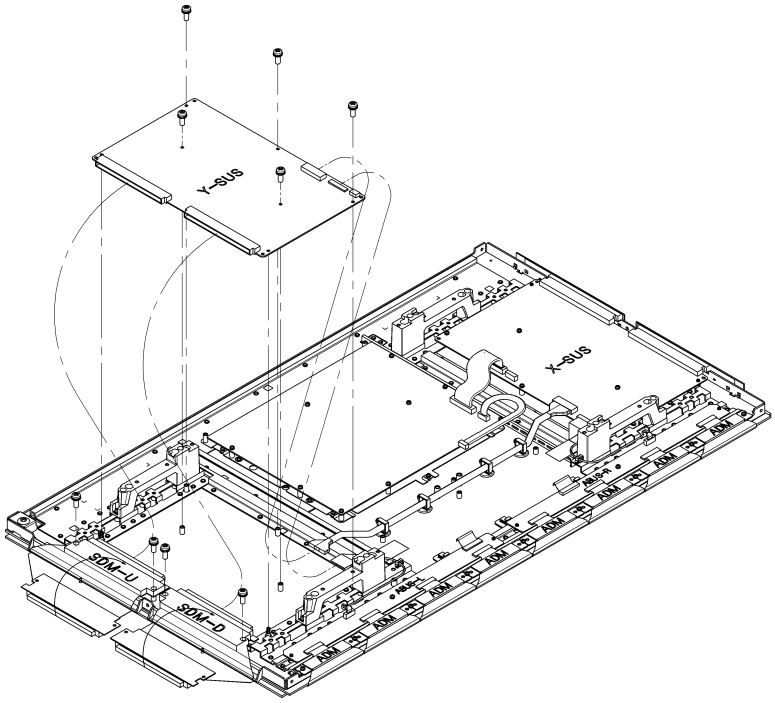
37A1_5. 1 DISASSEMBLE_LOGIC-L_1/2



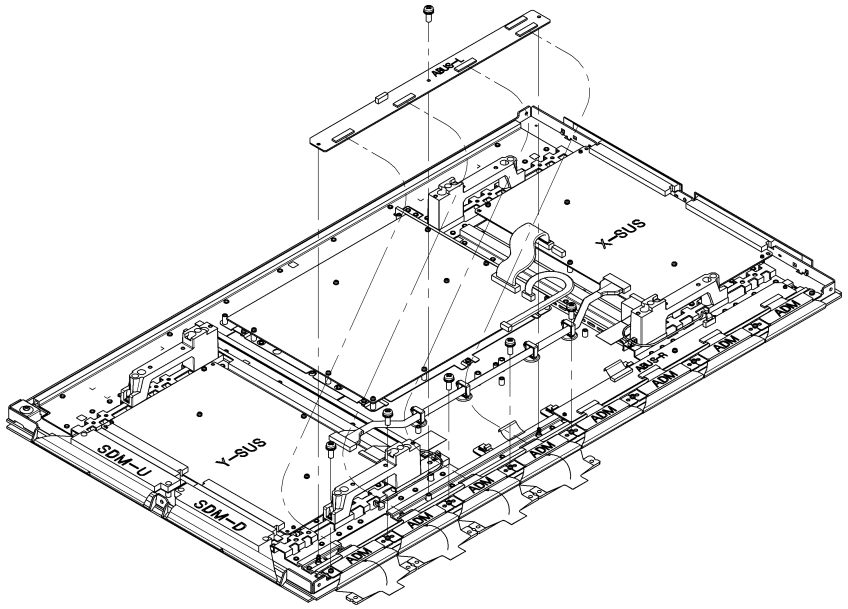
37A1_5. 1 DISASSEMBLE_LOGIC-L_2-2



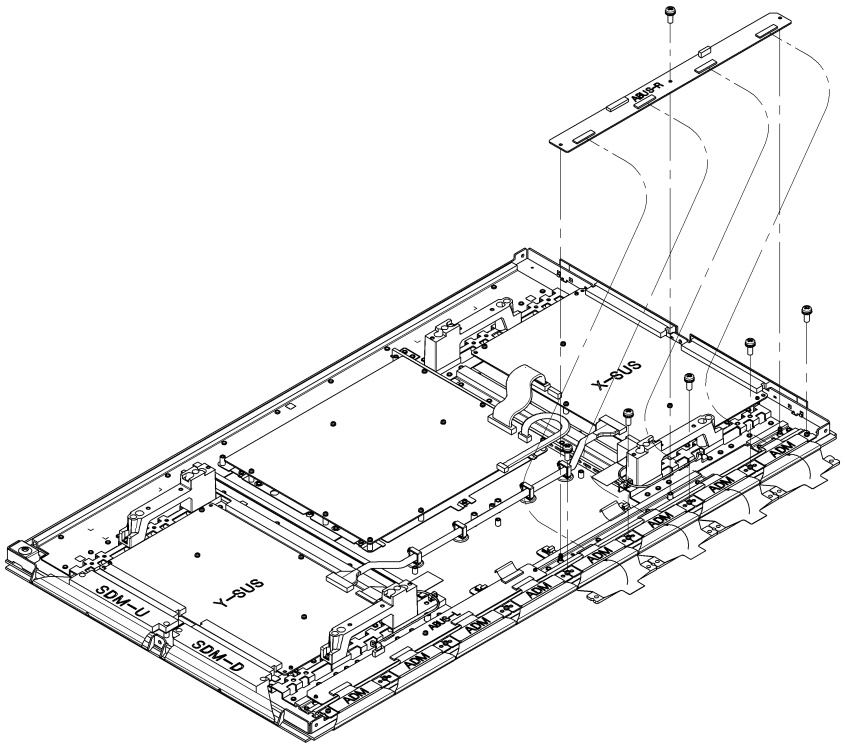
37A1_5. 2 (5) X-SUS



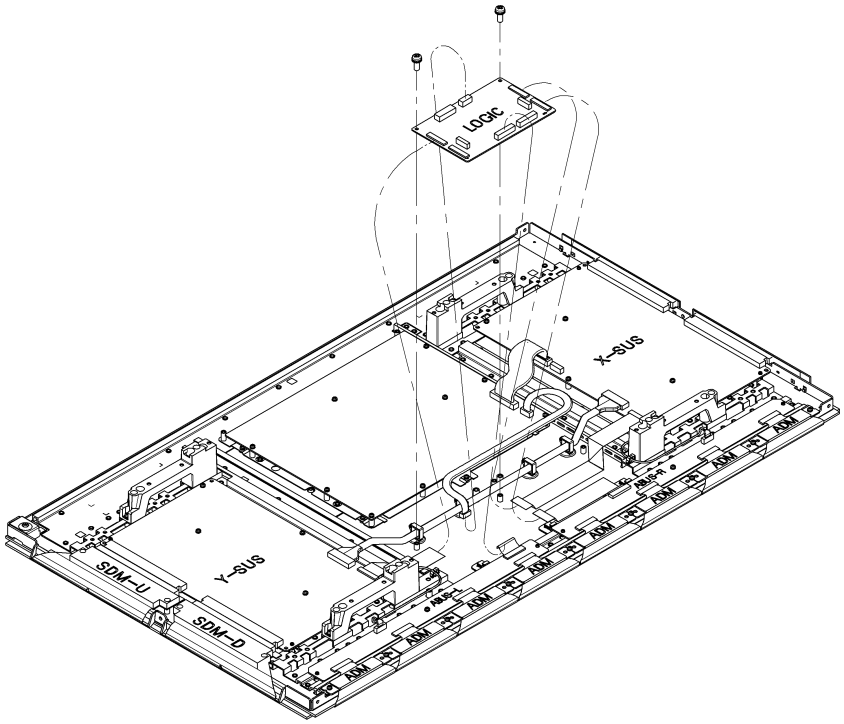
37A1_5. 3 (6) Y-SUS



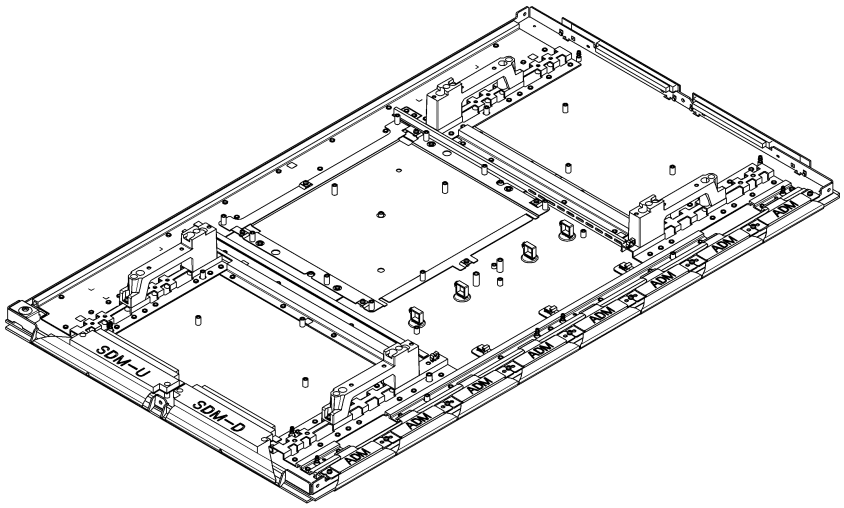
37A1_5. 4 (4)~(7) ADM, AbusL



37A1_5. 5 (4)~(7) ADM, AbusR



37A1_5. 6 (4)~(6) LOGIC-L



37A1_5. 8 COMPLETE PANEL CHASSIS REMOVAL

△1

8 THE PARTS INFORMATION

Module Repair Parts List

	Model name	Panel Module type	Part Number	Description	Note
1	KE-P37XS1 (AEP)	FPF37C128128UB-73	9-885-056-69	FPF22R-XSS0003	
2	KDE-P37XS1 (UK)		9-885-056-70	FPF22R-YSS0004	
3			9-885-056-71	FPF22R-LGC0004	
4			9-885-063-34	FPF22R-ABR0014	
5			9-885-063-35	FPF22R-ABL0013	
6			9-885-063-33	Panel module FPF37C128128UB-73	

	Model name	Panel Module type	Part Number	Description	Note
1	KE-P42XS1 (AEP)	FPF42C128128UC-53	9-885-056-75	FPF23R-XSS0005	
2	KDE-P42XS1 (UK)		9-885-056-76	FPF23R-YSS0006	
3	KE-MX42A1 (HK), (ME)		9-885-056-77	FPF23R-LGC0006	
4	KE-MX42S1 (OCE)		9-885-056-78	FPF23R-ABR0002	
5			9-885-056-79	FPF23R-ABL0001	
6			9-885-059-67	Panel module FPF42C128128UC-53	

	Model name	Panel Module type	Part Number	Description	Note
1	KE-MX42M1 (CH)	FPF42C128128UC-59	9-885-056-75	FPF23R-XSS0005	
2			9-885-056-76	FPF23R-YSS0006	
3			9-885-056-77	FPF23R-LGC0006	
4			9-885-056-78	FPF23R-ABR0002	
5			9-885-056-79	FPF23R-ABL0001	
6			9-885-068-67	Panel module FPF42C128128UC-59	(for CH only)

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Sony EMCS Corporation
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